Fig. 1

PRIOR ART

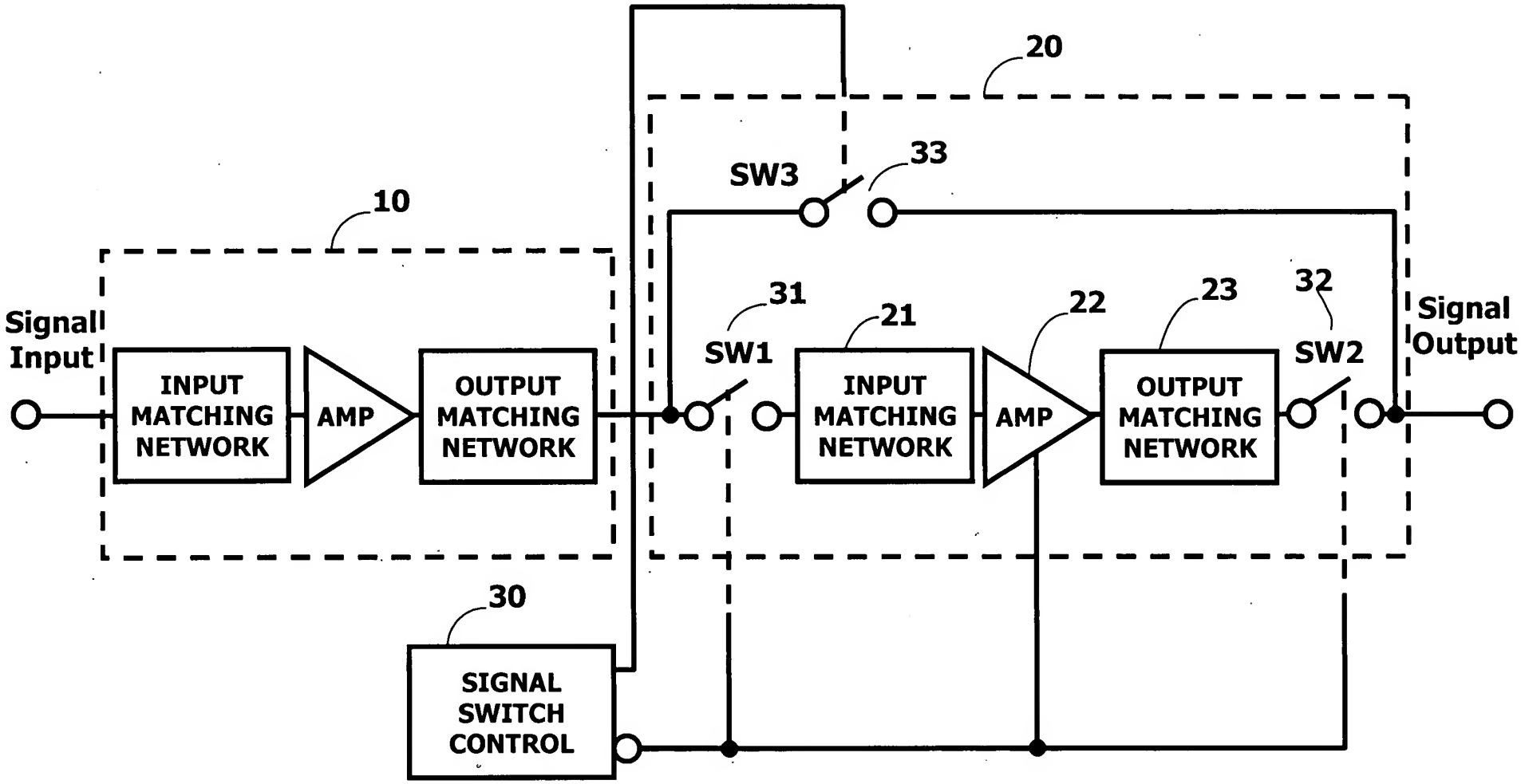
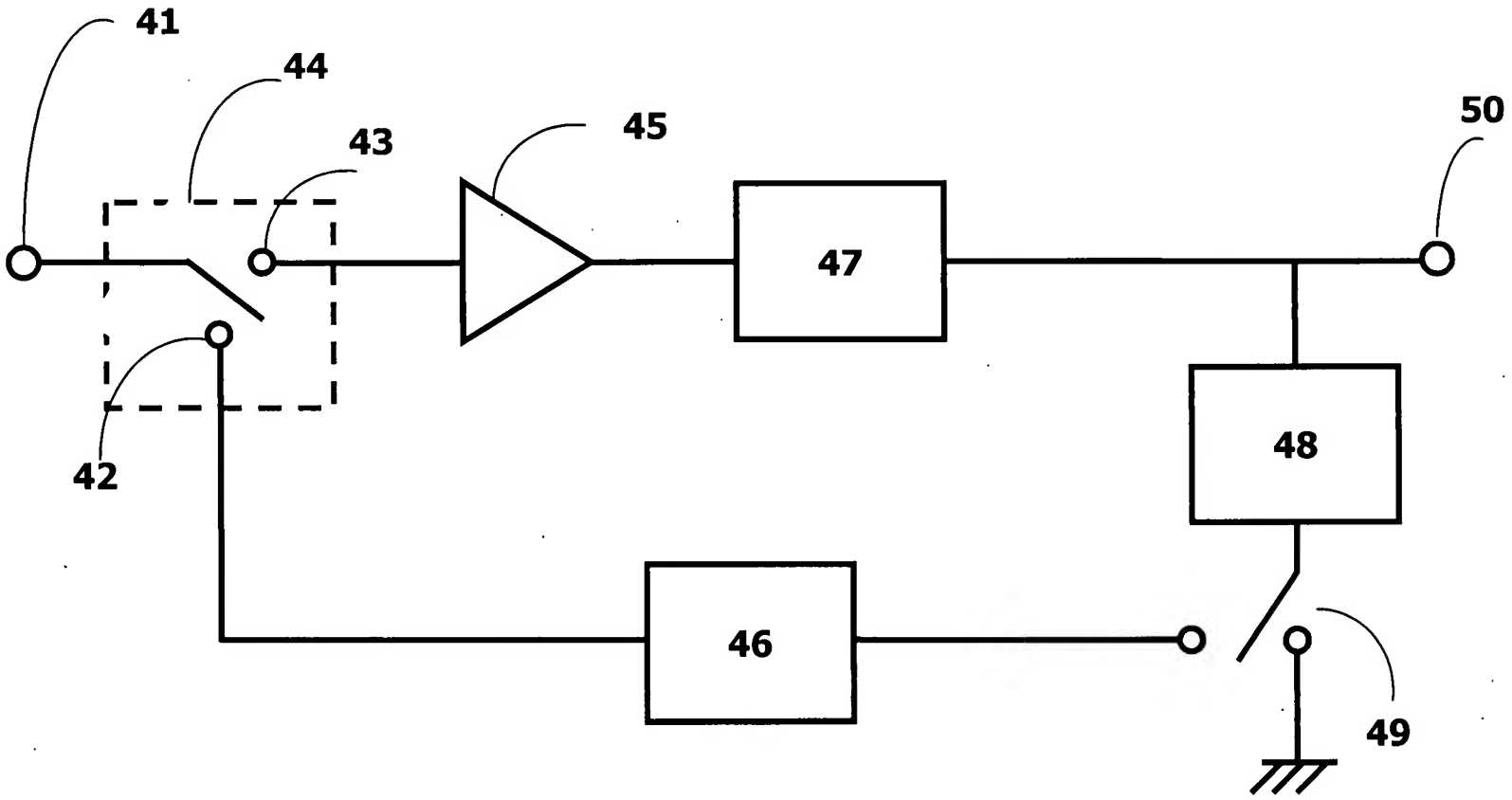


Fig. 2

PRIOR ART



PRIOR ART

Fig. 3A

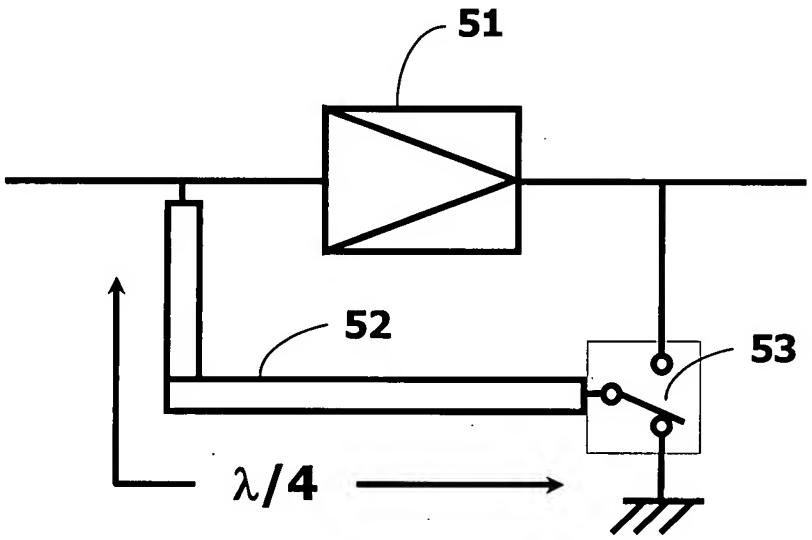
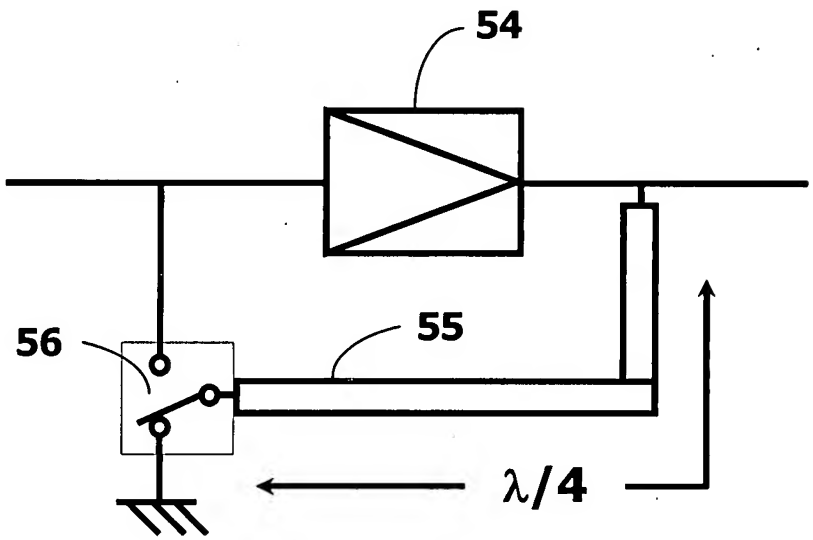


Fig. 3B



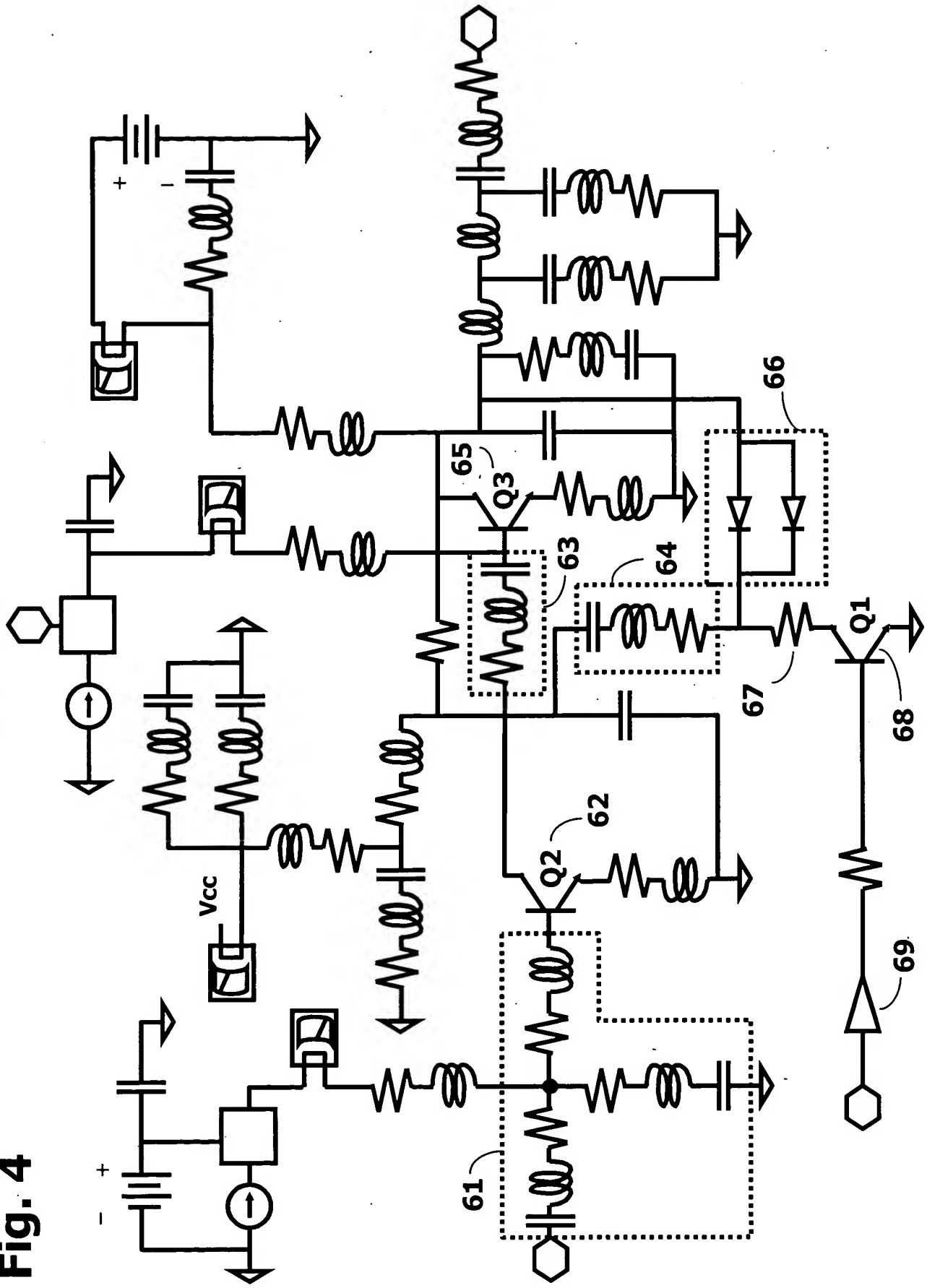


Fig. 4

Fig. 5

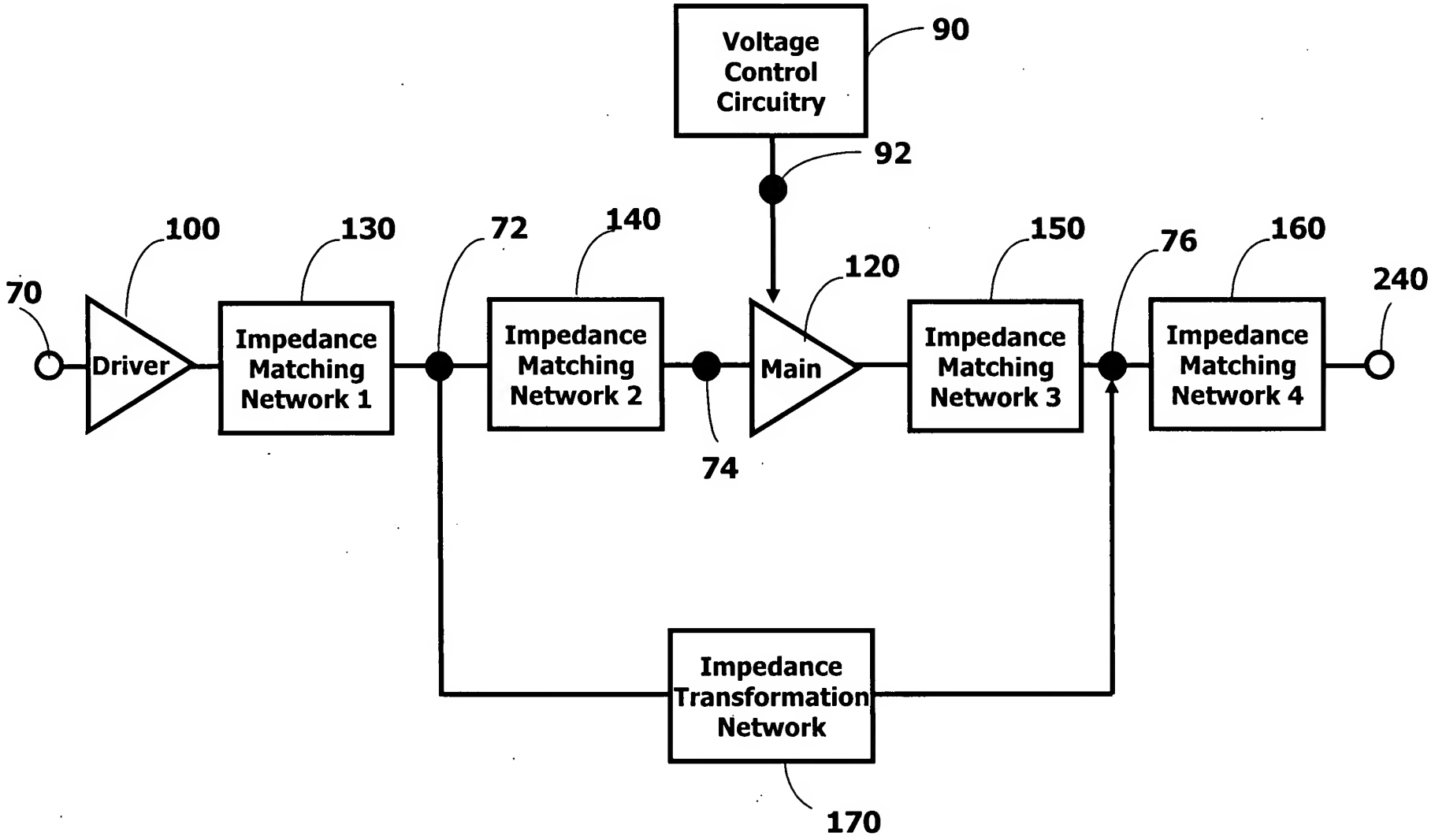

Voltage Control Circuitry
90
92
100
130
72
140
120
150
76
160
240
70
Driver
Impedance Matching Network 1
Impedance Matching Network 2
Main
Impedance Matching Network 3
Impedance Matching Network 4
74
Impedance Transformation Network
170

Fig. 6

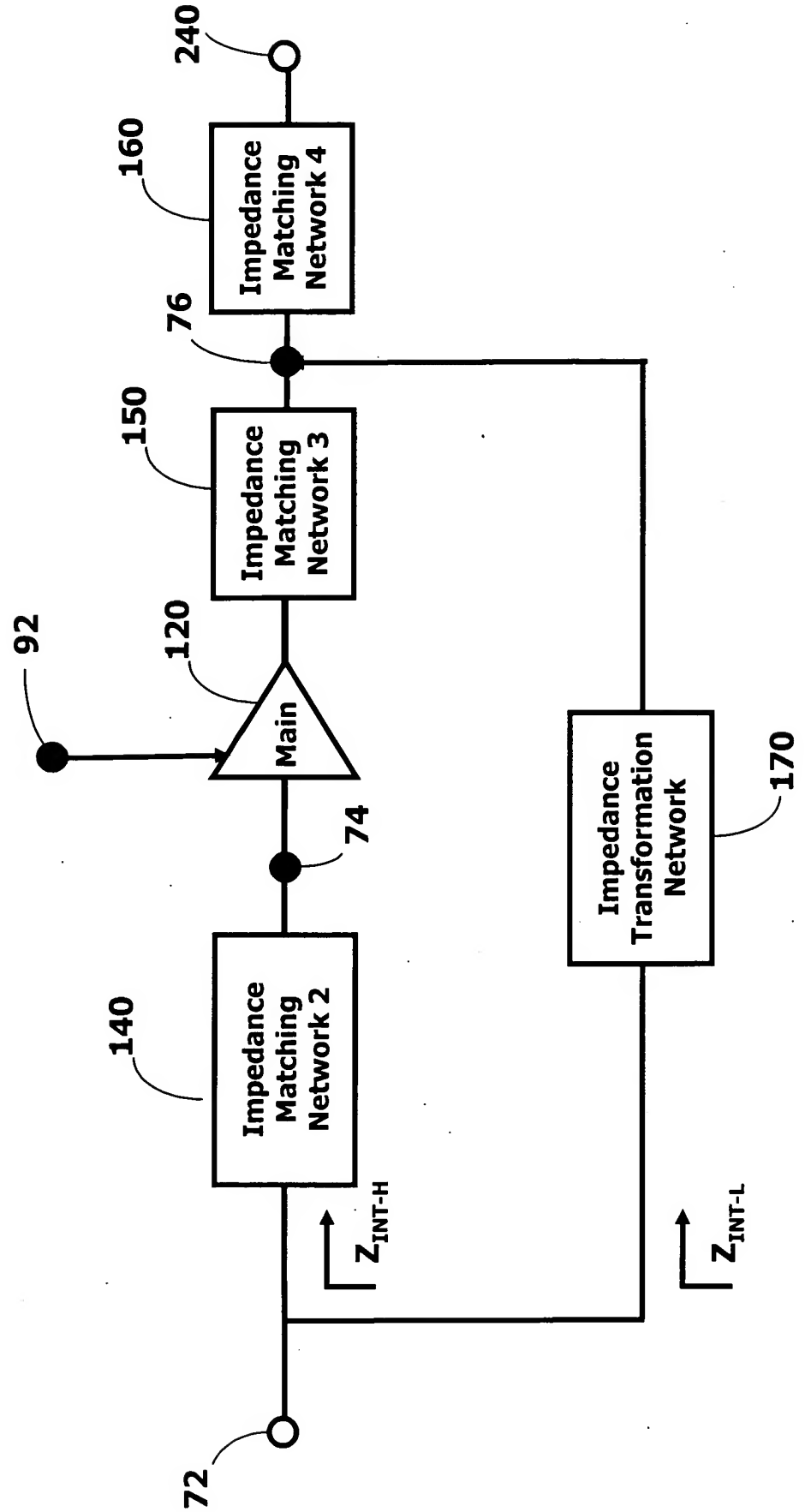

240
160
Impedance Matching Network 4
76
150
Impedance Matching Network 3
92
120
Main
74
140
Impedance Matching Network 2
72
Impedance Transformation Network
170
Z_{INT-H}
Z_{INT-L}

Fig. 7A

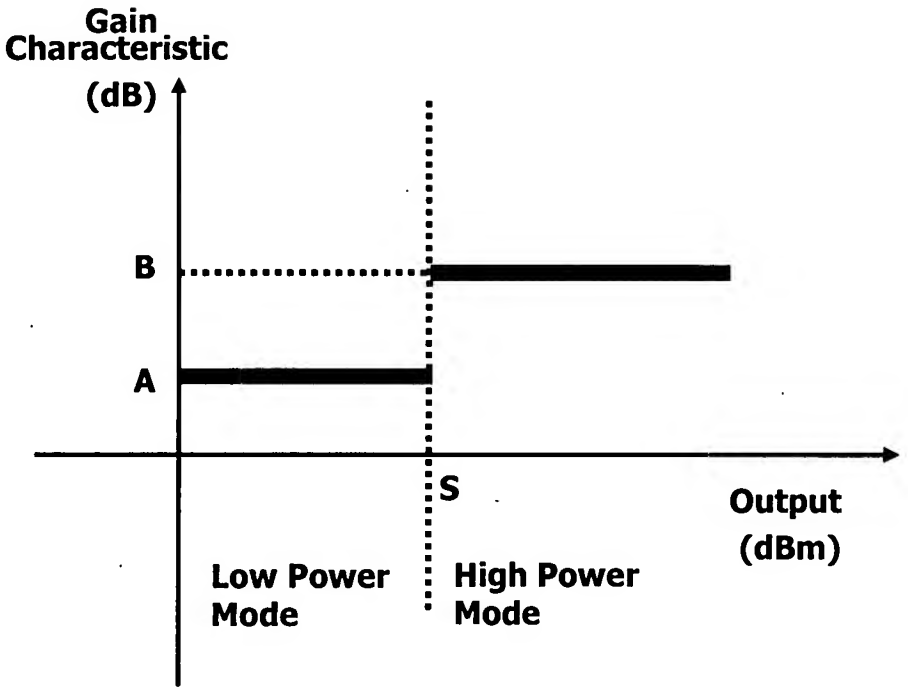

Gain
Characteristic
(dB)
B
A
S
Output
(dBm)
Low Power
Mode
High Power
Mode

Fig. 7B

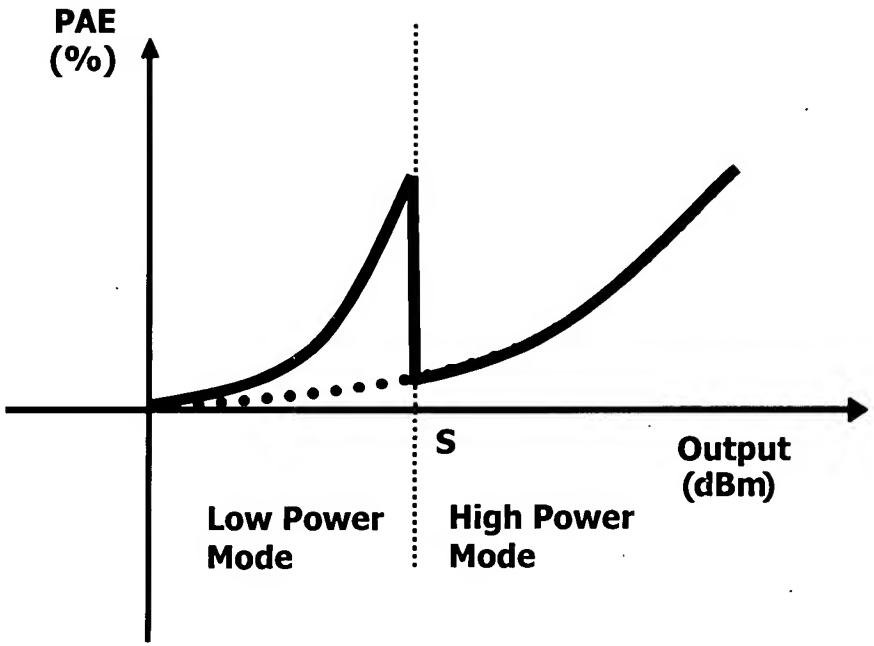

PAE
(%)
S
Output
(dBm)
Low Power
Mode
High Power
Mode

Fig. 8

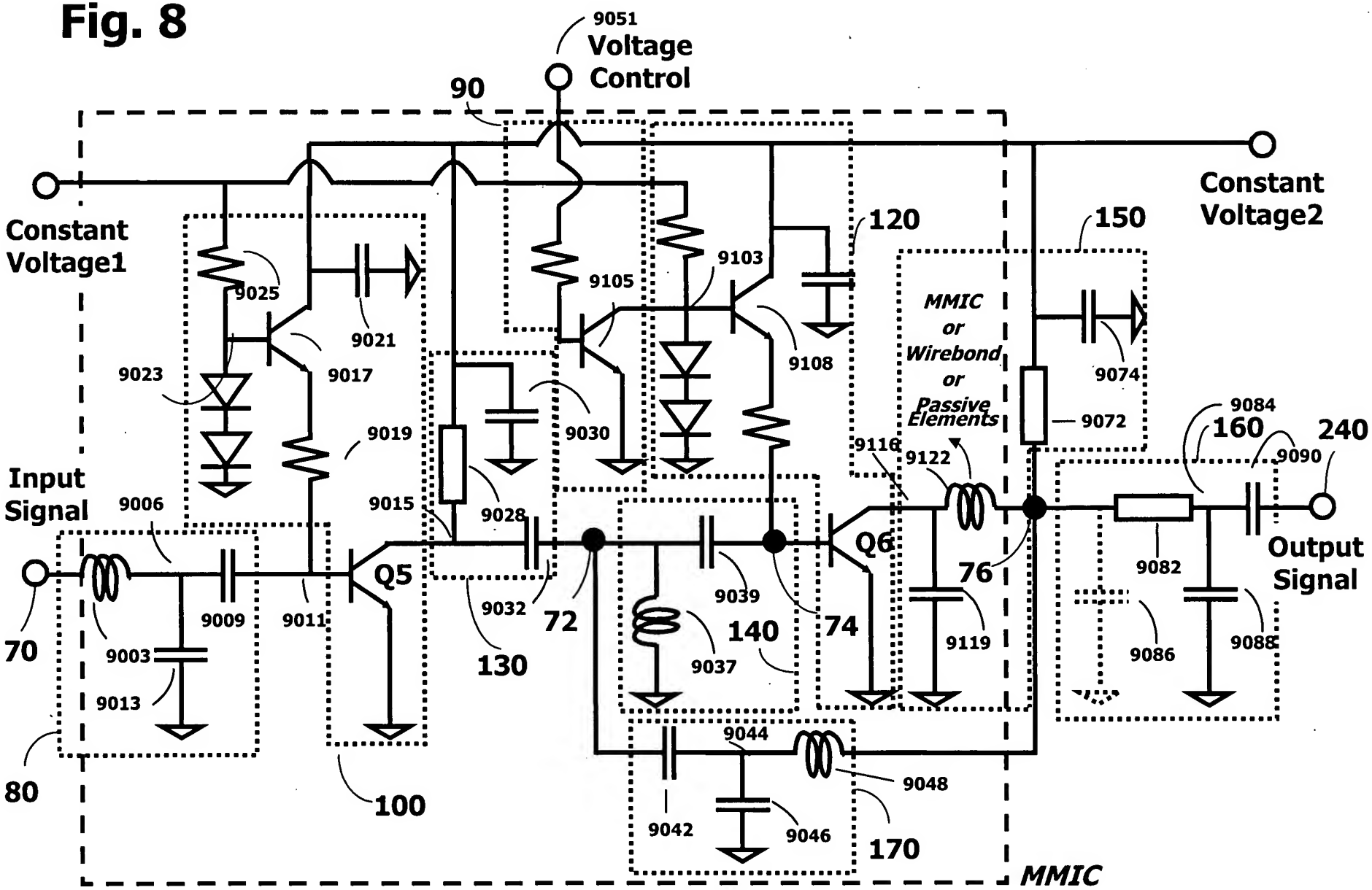

9051
Voltage
Control
90
Constant
Voltage1
Constant
Voltage2
120
150
9103
9105
9025
9021
9023
9017
9108
9074
MMIC
or
Wirebond
or
Passive
Elements
9072
9084
160
240
9090
9116
9122
9019
9030
Input
Signal
9006
9015
9028
Q6
Q5
76
9082
Output
Signal
9009
9011
9039
9032
72
74
9119
70
9003
9037
140
9086
9088
130
9013
9044
9048
80
100
9042
9046
170
MMIC

Fig. 9

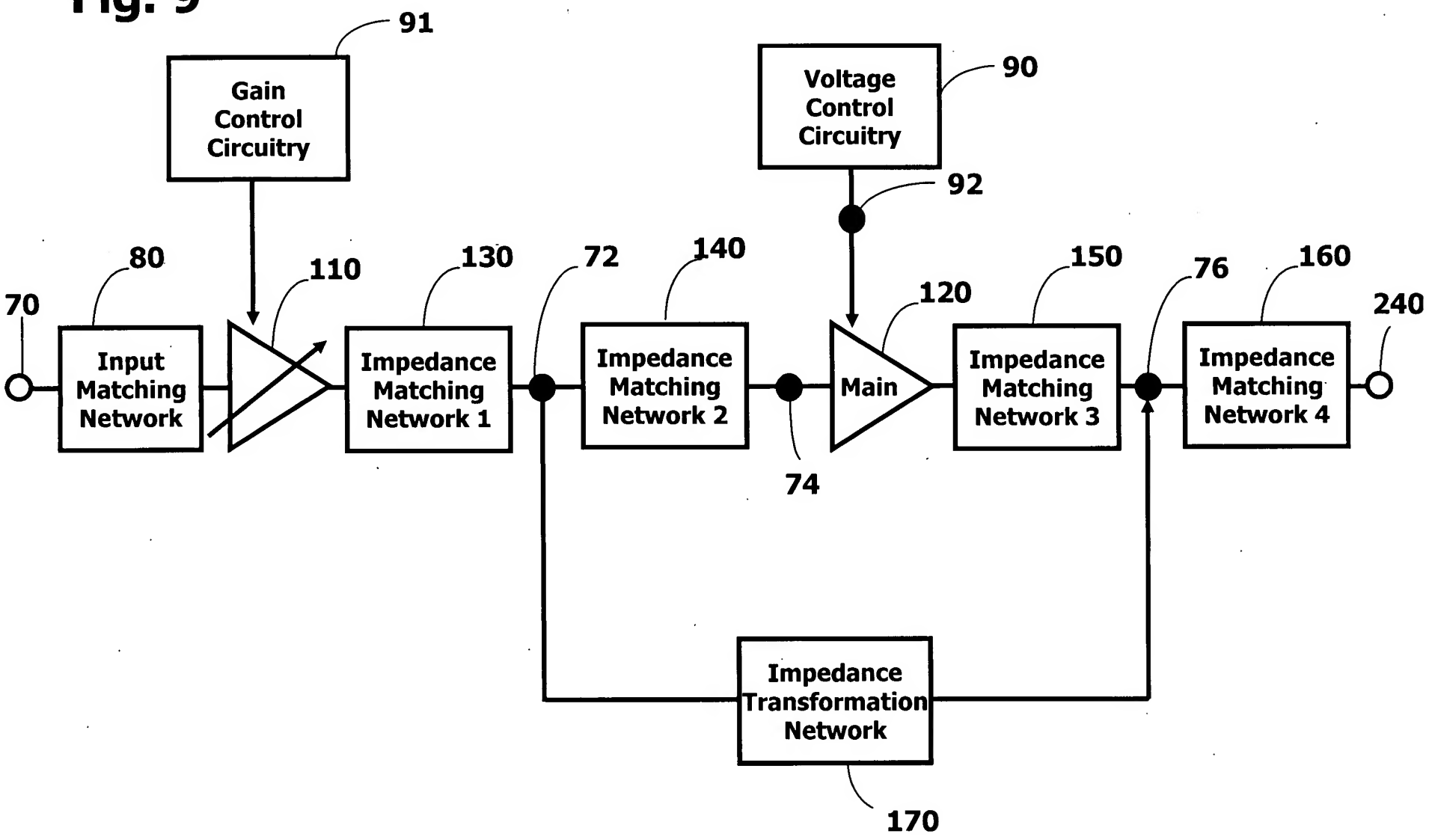

91
Gain Control Circuitry
90
Voltage Control Circuitry
92
80
110
130
72
140
120
150
76
160
70
240
Input Matching Network
Impedance Matching Network 1
Impedance Matching Network 2
Main
Impedance Matching Network 3
Impedance Matching Network 4
74
Impedance Transformation Network
170

Fig. 10

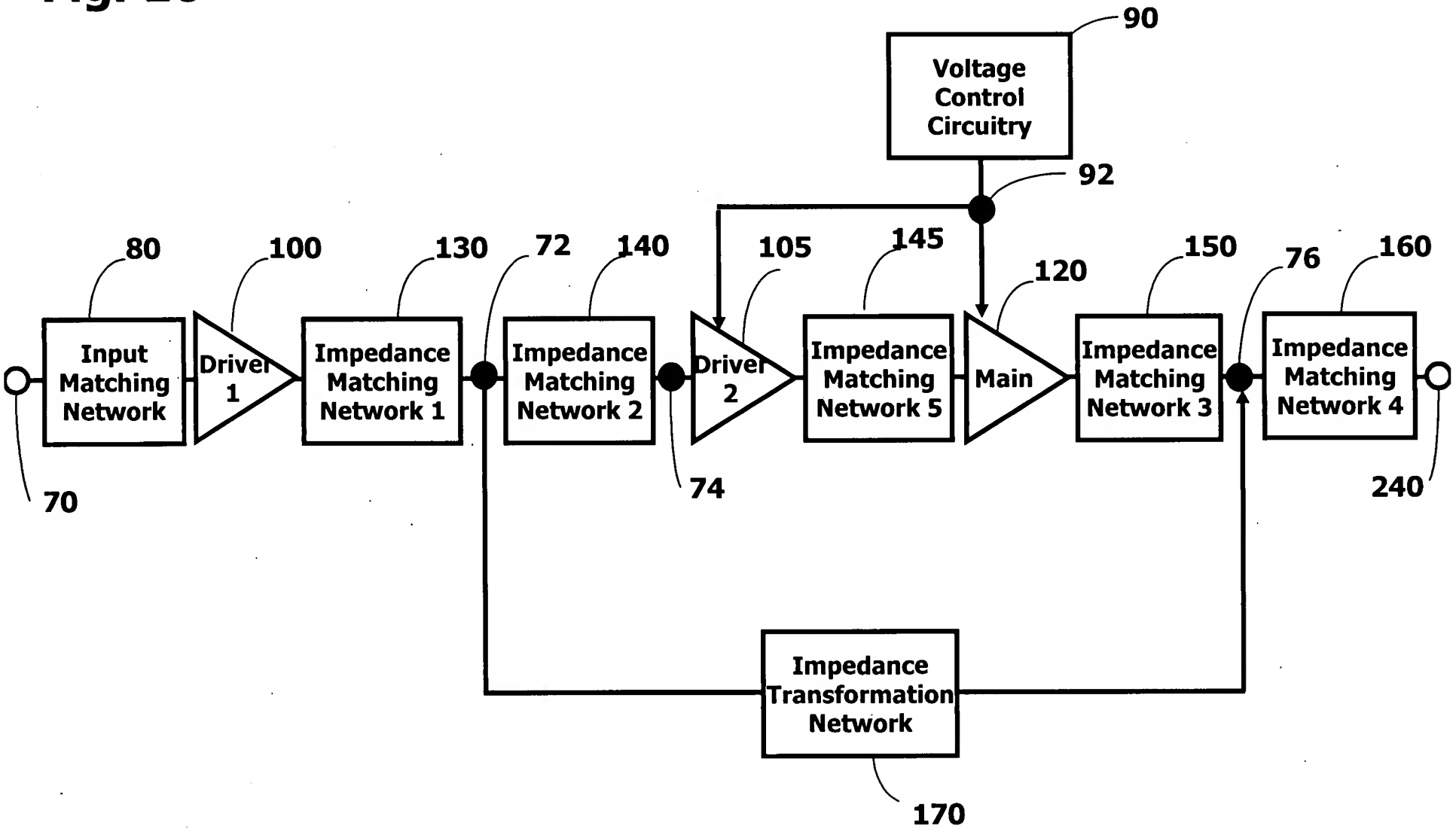

90
Voltage Control Circuitry
92
80
100
130
72
140
105
145
120
150
76
160
Input Matching Network
Driver 1
Impedance Matching Network 1
Impedance Matching Network 2
Driver 2
Impedance Matching Network 5
Main
Impedance Matching Network 3
Impedance Matching Network 4
70
74
240
Impedance Transformation Network
170

Fig. 11

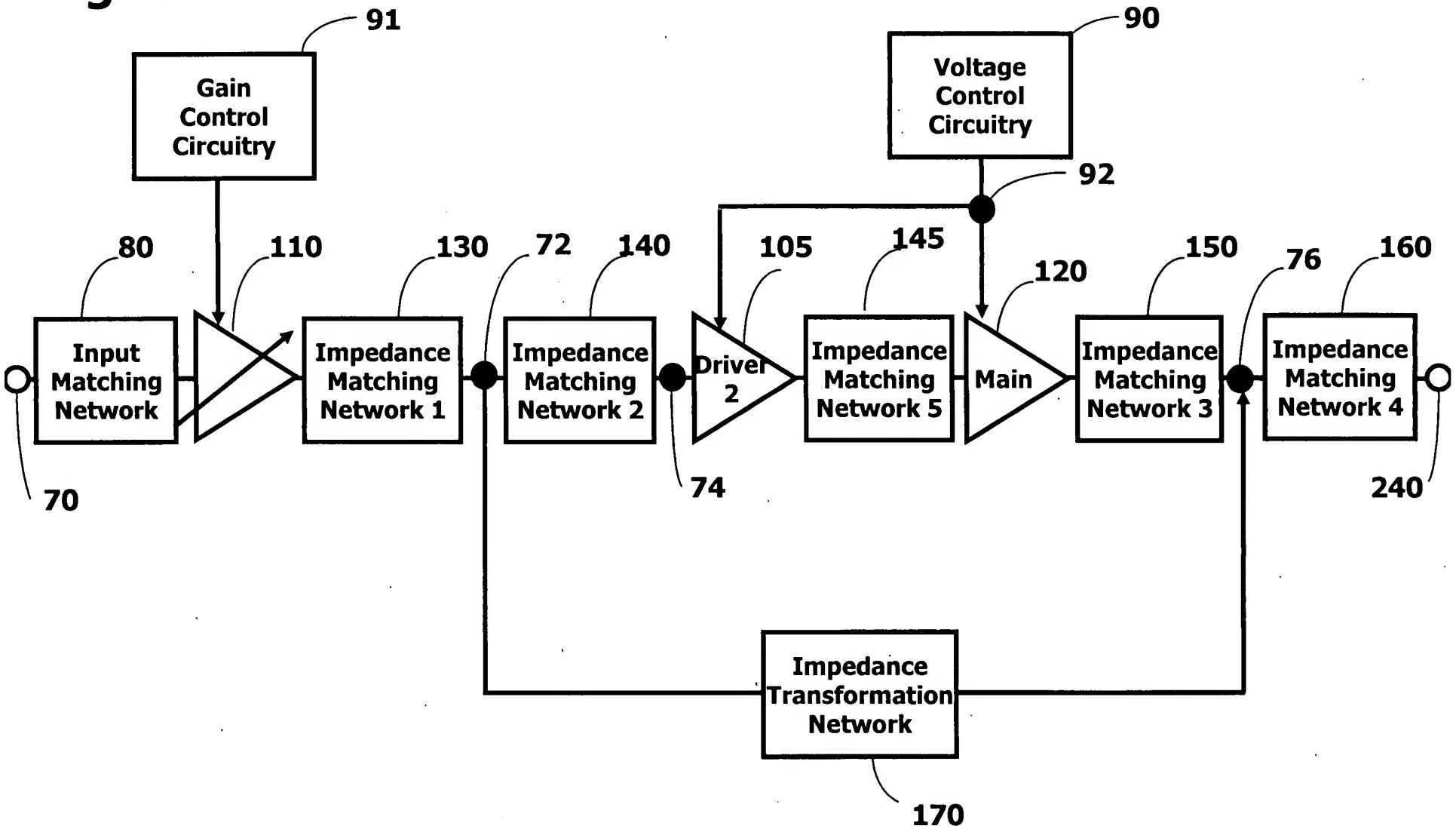

91
Gain Control Circuitry
90
Voltage Control Circuitry
92
80
110
130
72
140
105
145
120
150
76
160
Input Matching Network
Impedance Matching Network 1
Impedance Matching Network 2
Driver 2
Impedance Matching Network 5
Main
Impedance Matching Network 3
Impedance Matching Network 4
70
74
240
Impedance Transformation Network
170

Fig. 12

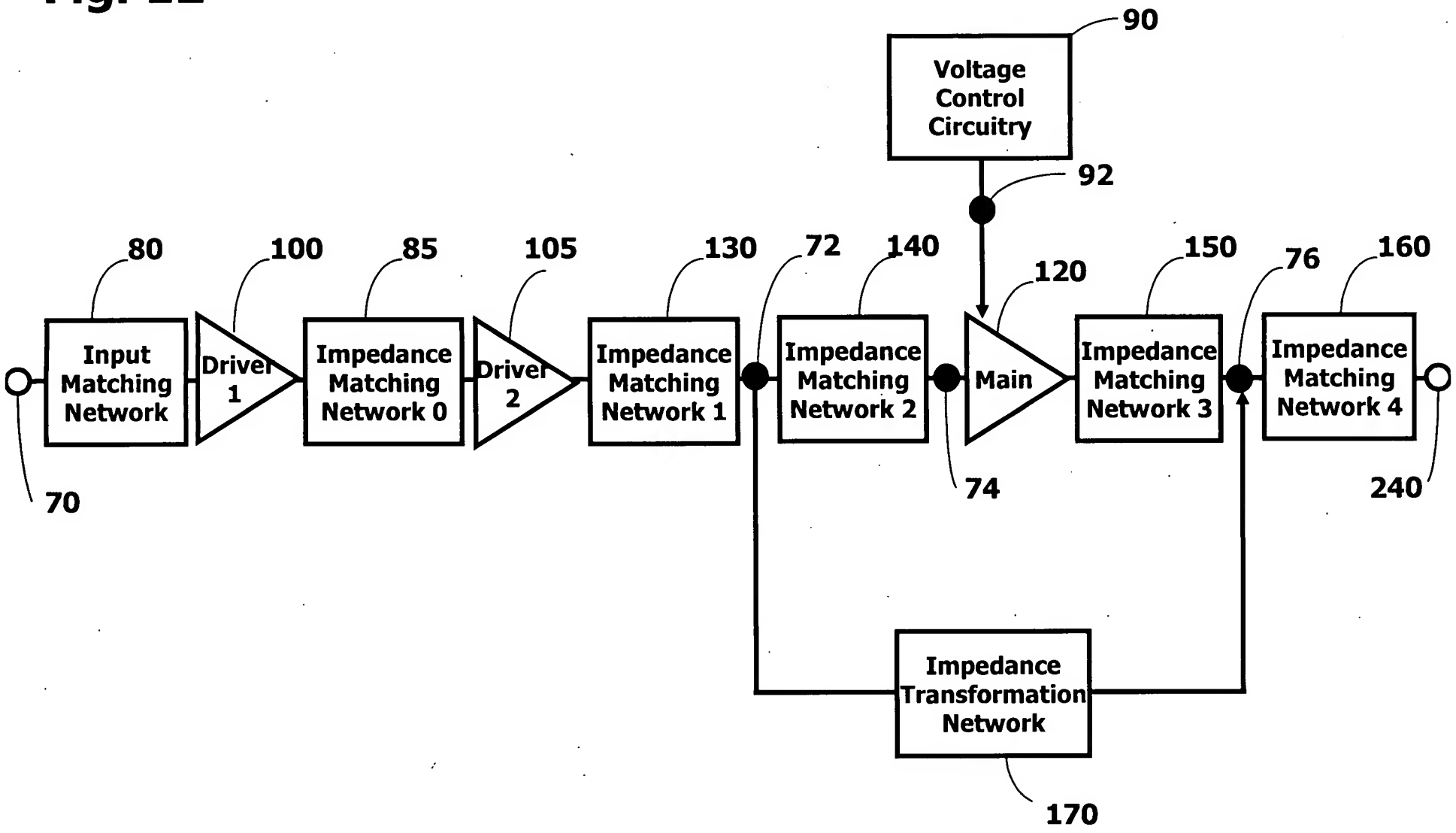

90
Voltage Control Circuitry
92
80
100
85
105
130
72
140
120
150
76
160
Input Matching Network
Driver 1
Impedance Matching Network 0
Driver 2
Impedance Matching Network 1
Impedance Matching Network 2
Main
Impedance Matching Network 3
Impedance Matching Network 4
70
74
240
Impedance Transformation Network
170

Fig. 13

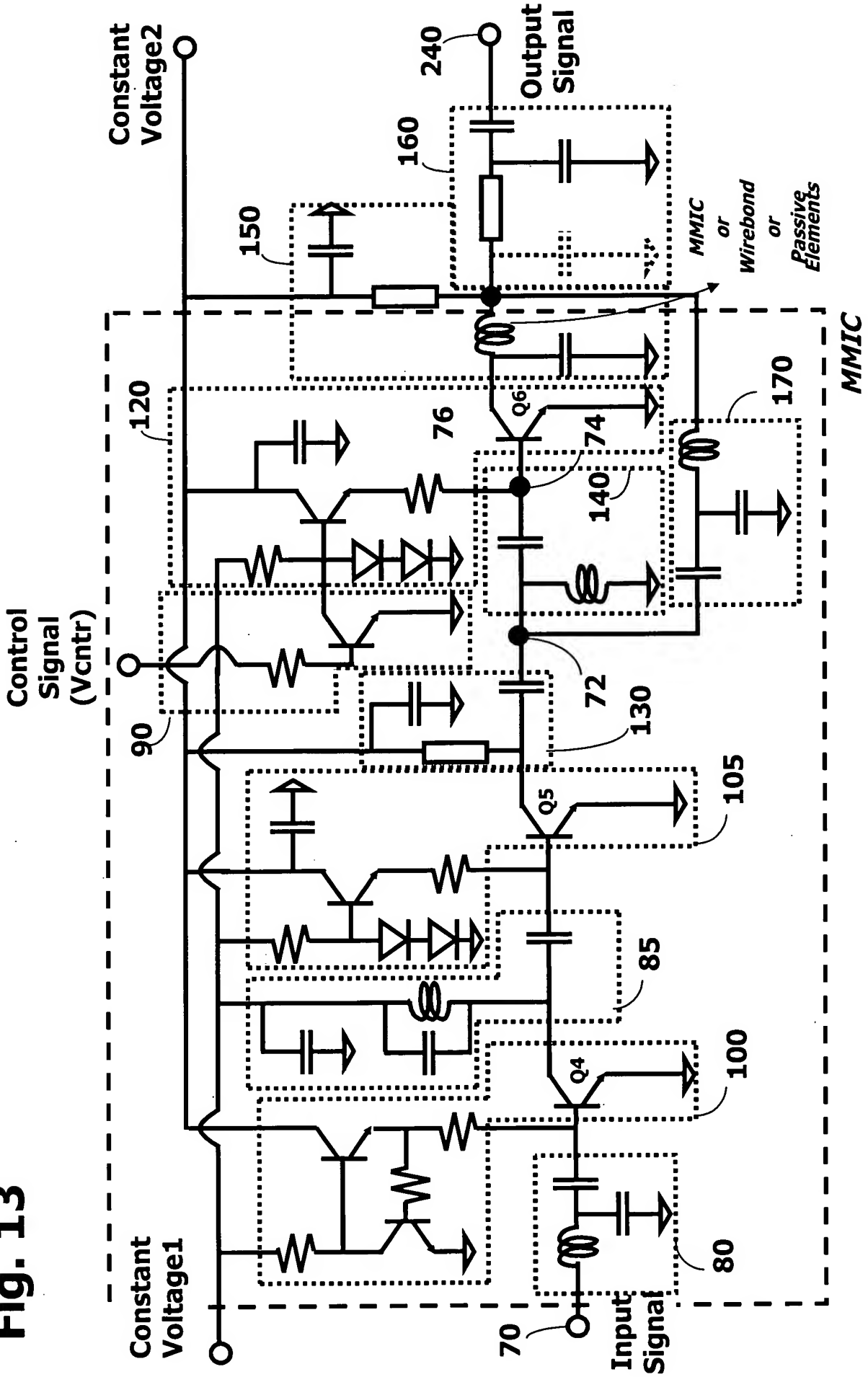

Constant Voltage2
Output Signal
240
160
150
MMIC or Wirebond or Passive Elements
MMIC
120
76
Q6
74
170
140
Control Signal (Vcntr)
90
72
130
105
Q5
85
100
Q4
Constant Voltage1
70
Input Signal
80

Fig. 14

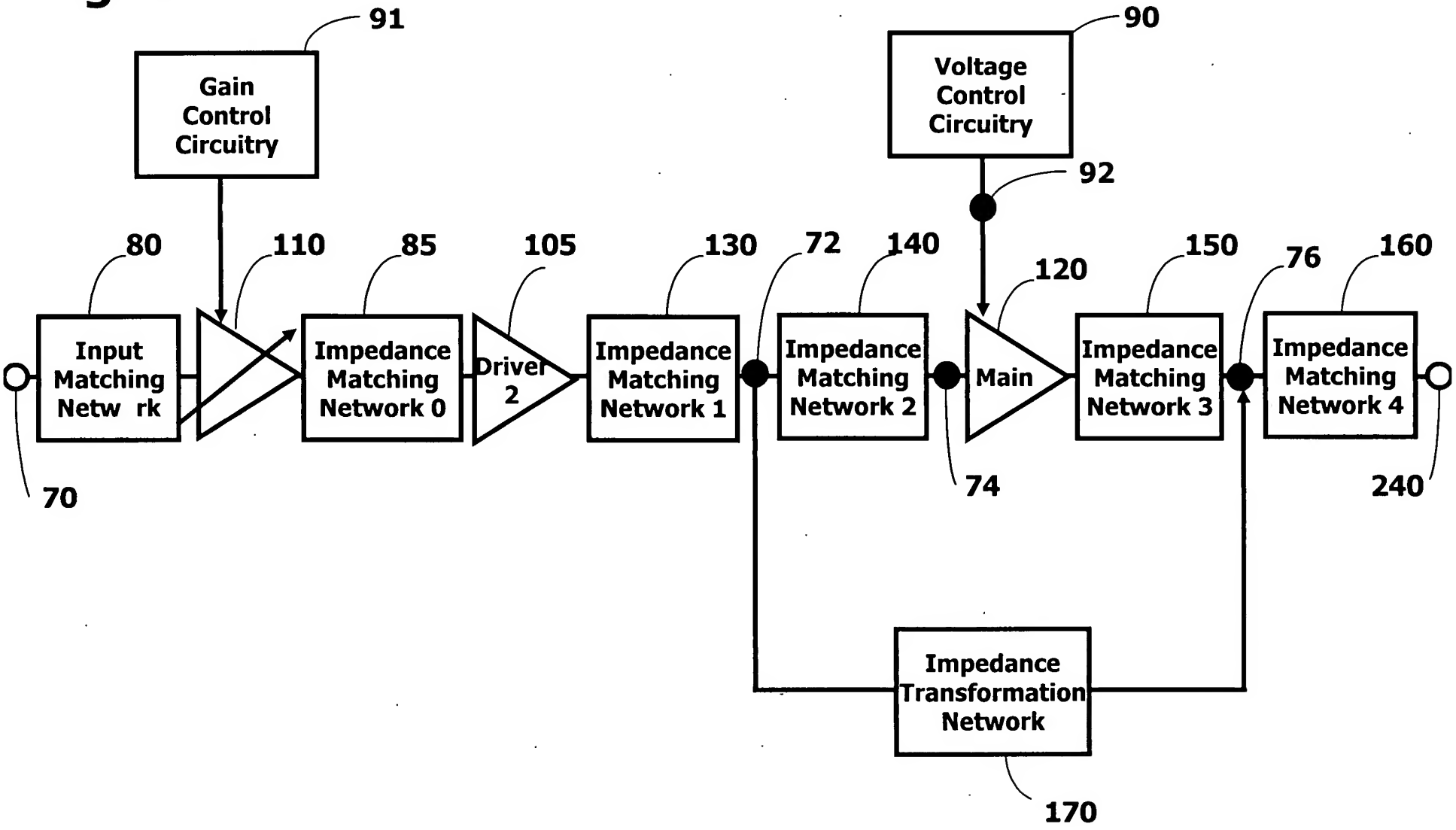
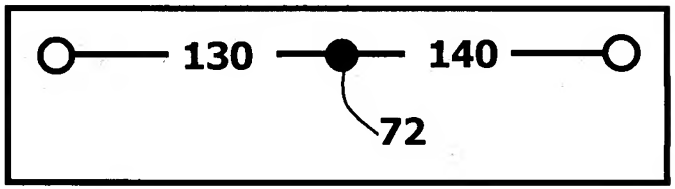
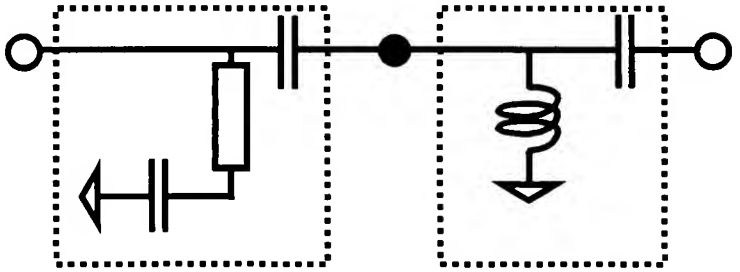

91
Gain Control Circuitry
90
Voltage Control Circuitry
92
80
110
85
105
130
72
140
120
150
76
160
Input Matching Netw rk
Impedance Matching Network 0
Driver 2
Impedance Matching Network 1
Impedance Matching Network 2
Main
Impedance Matching Network 3
Impedance Matching Network 4
70
74
240
Impedance Transformation Network
170

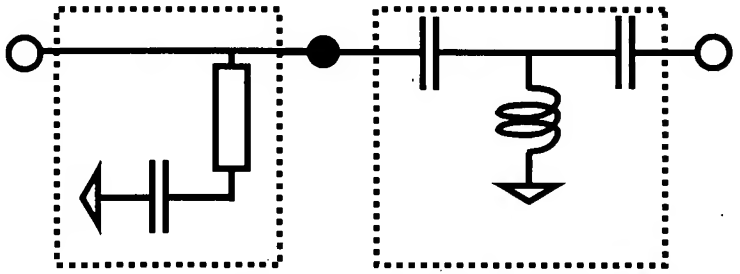
Fig. 15



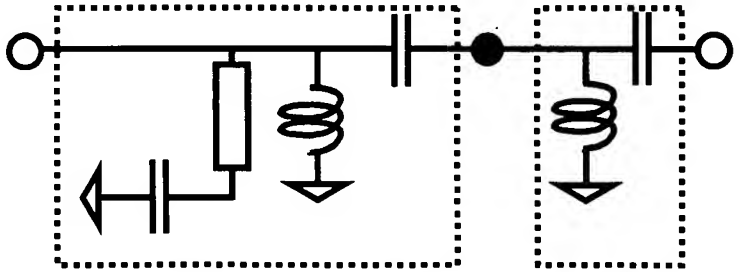
15-1



15-2



15-3



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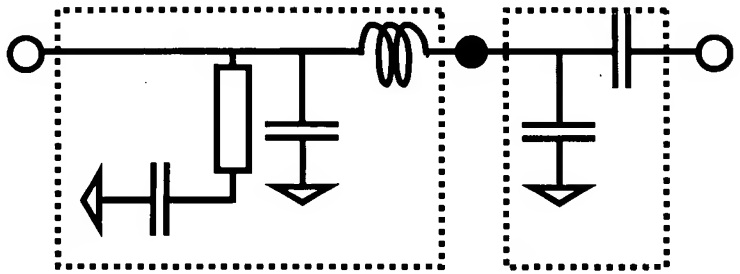

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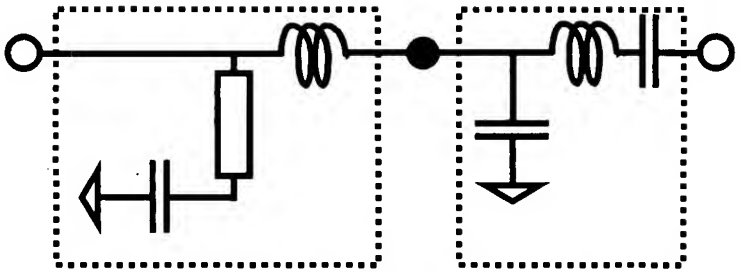
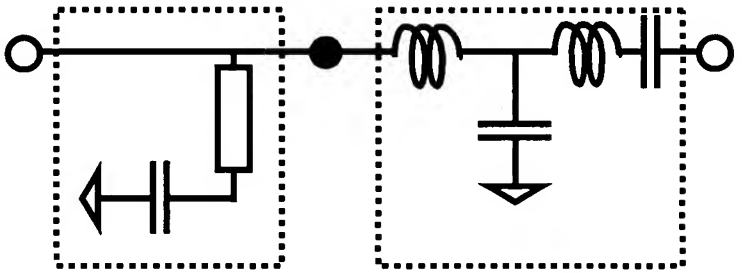


15-6



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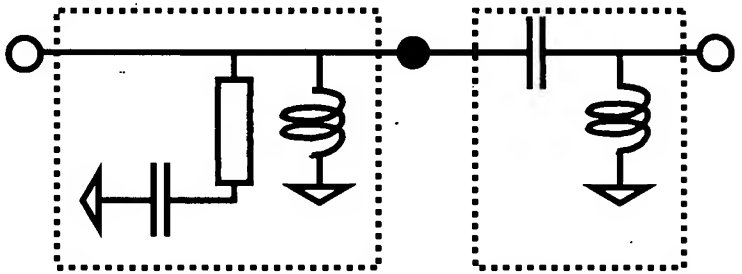


15-8

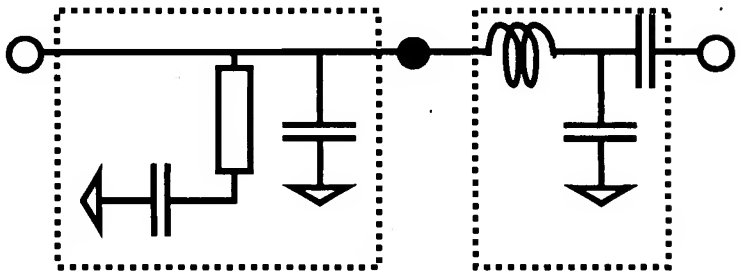
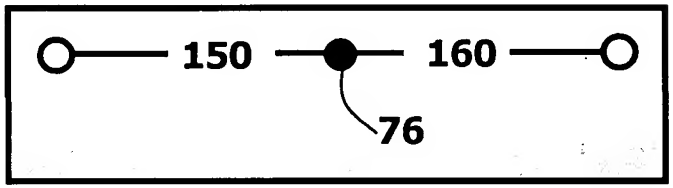
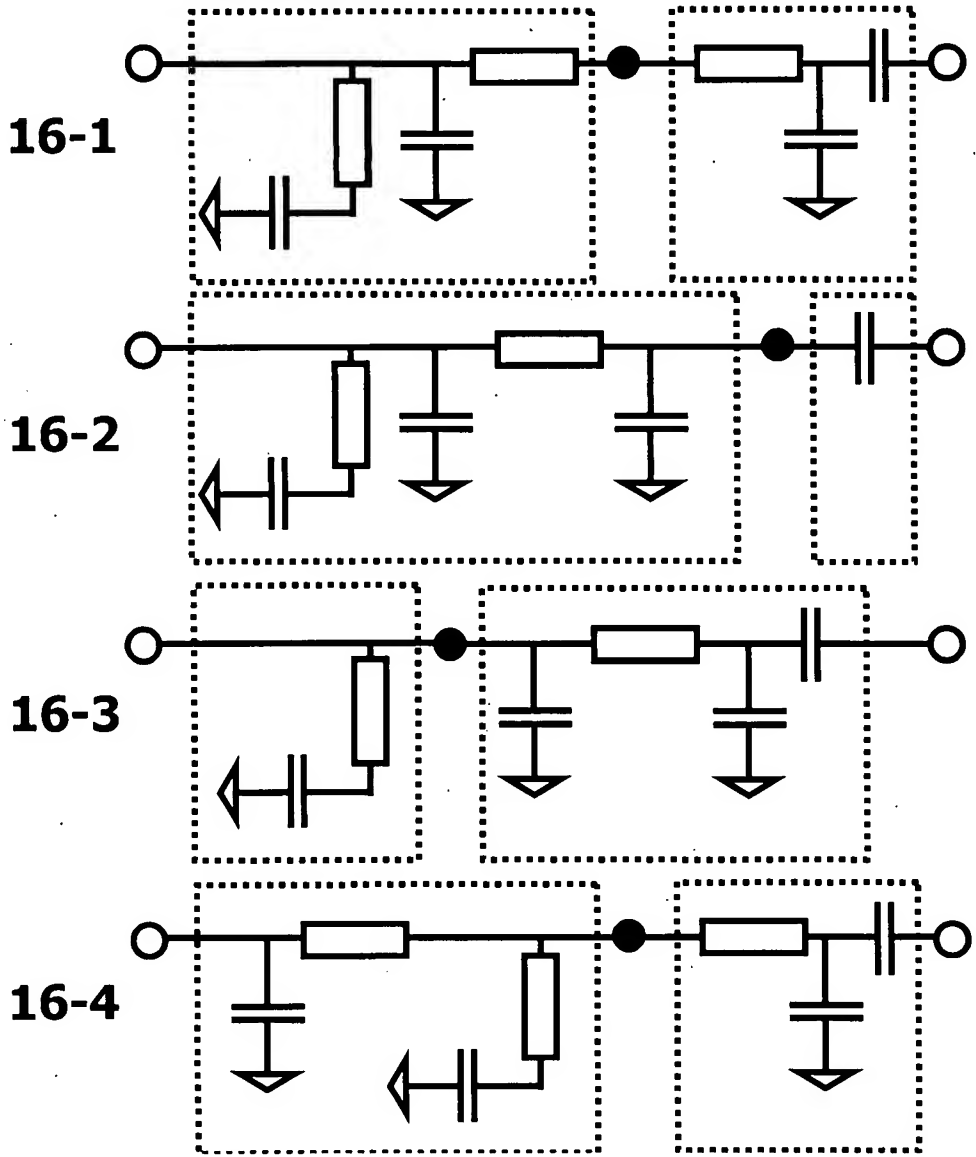


Fig. 16





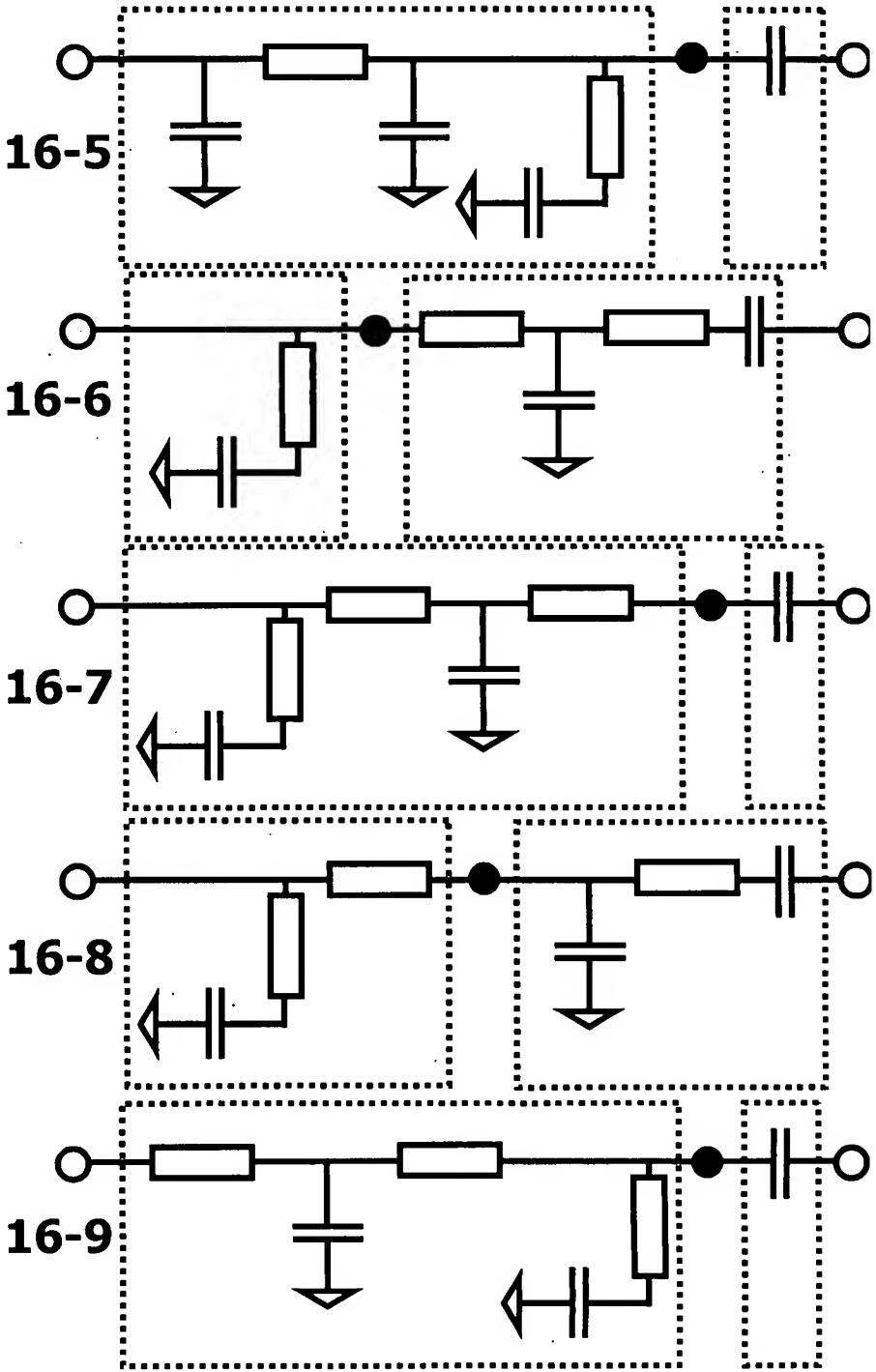
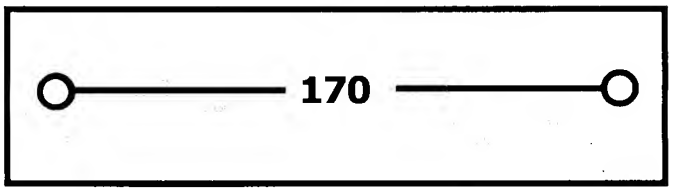
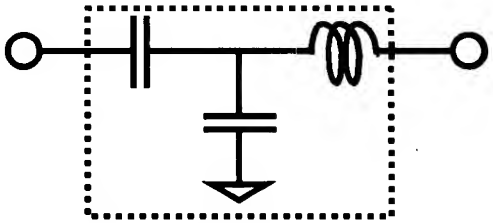


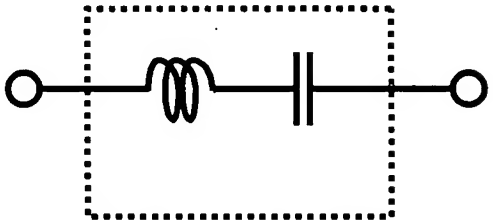
Fig. 17



17-1



17-2



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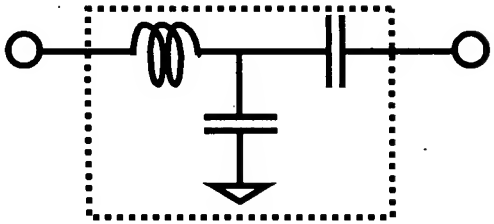

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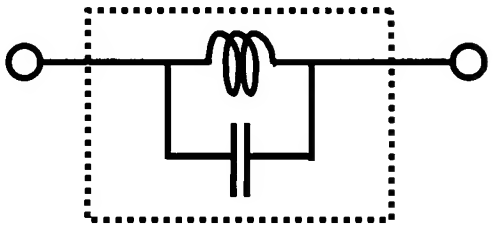
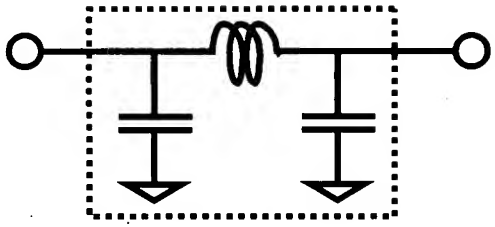


17-5



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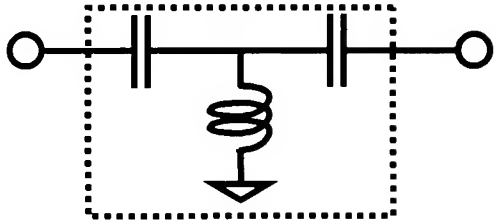

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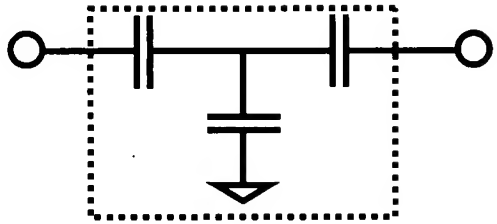


17-8

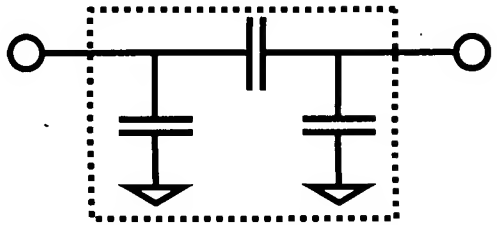


Fig. 18

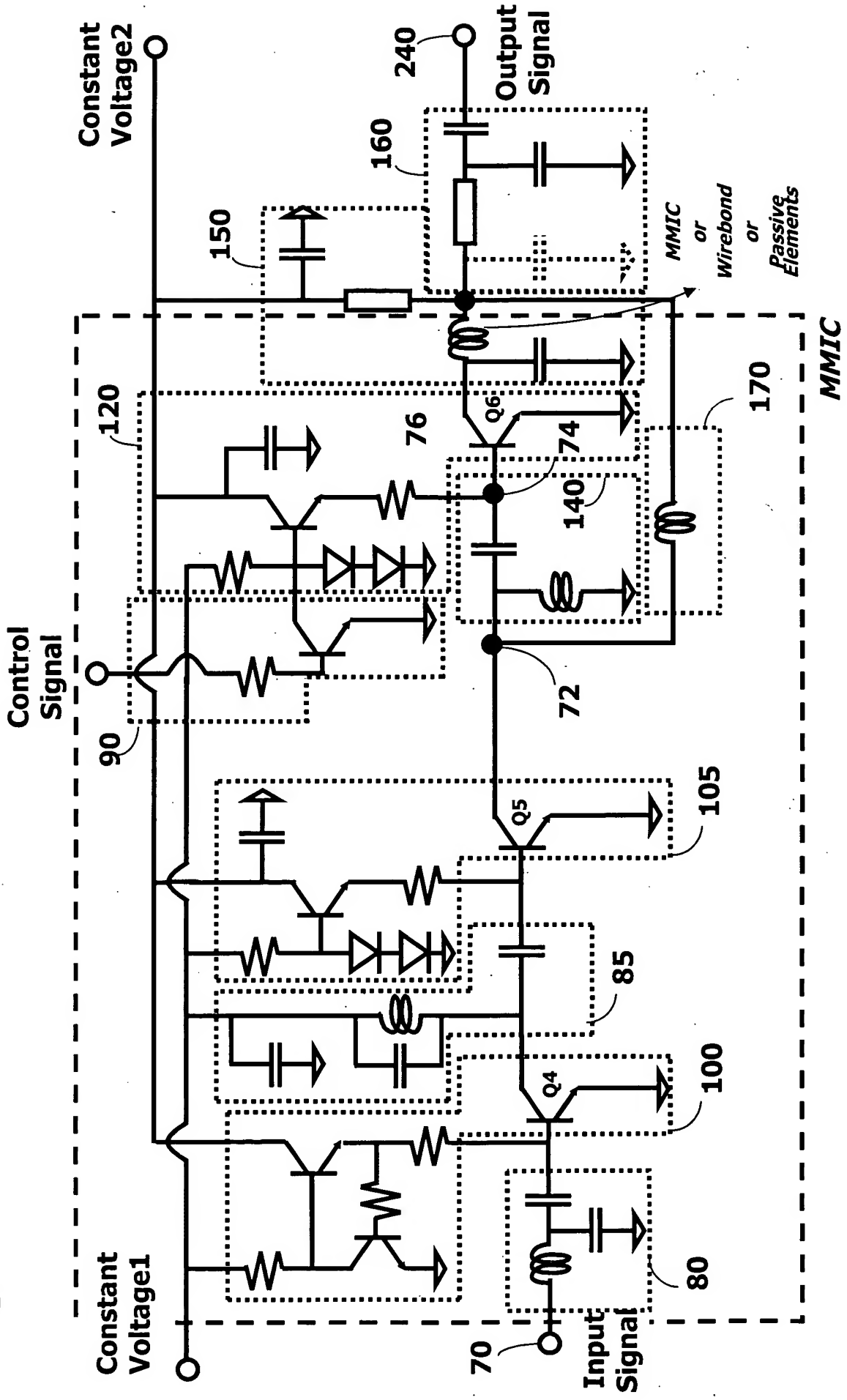
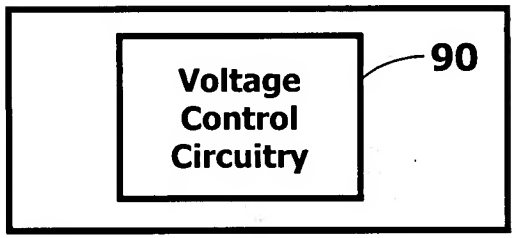
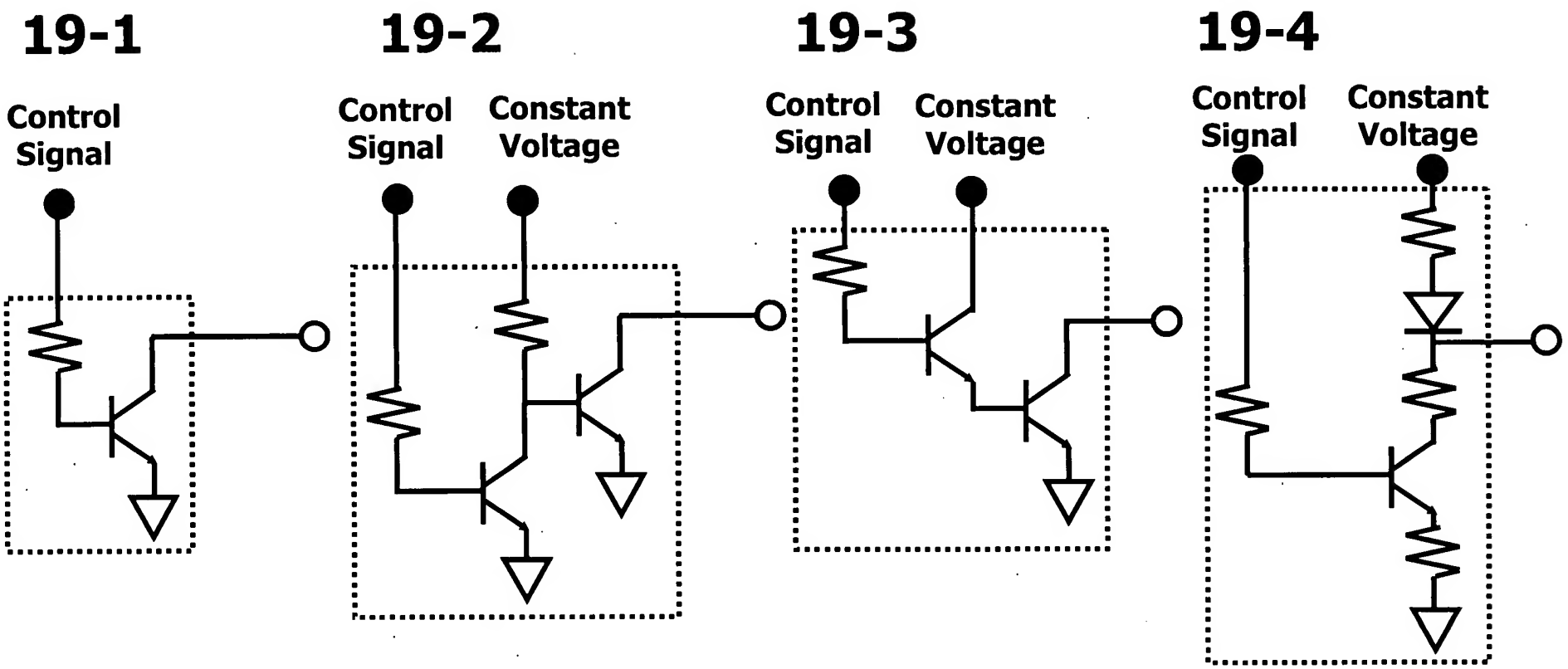

Constant Voltage2
240
Output Signal
160
150
MMIC or Wirebond or Passive Elements
MMIC
120
170
Q6
76
74
140
72
Control Signal
90
105
Q5
85
100
Q4
80
Constant Voltage1
70
Input Signal

Fig. 19


Voltage
Control
Circuitry
90


19-1
Control
Signal
19-2
Control
Signal
Constant
Voltage
19-3
Control
Signal
Constant
Voltage
19-4
Control
Signal
Constant
Voltage

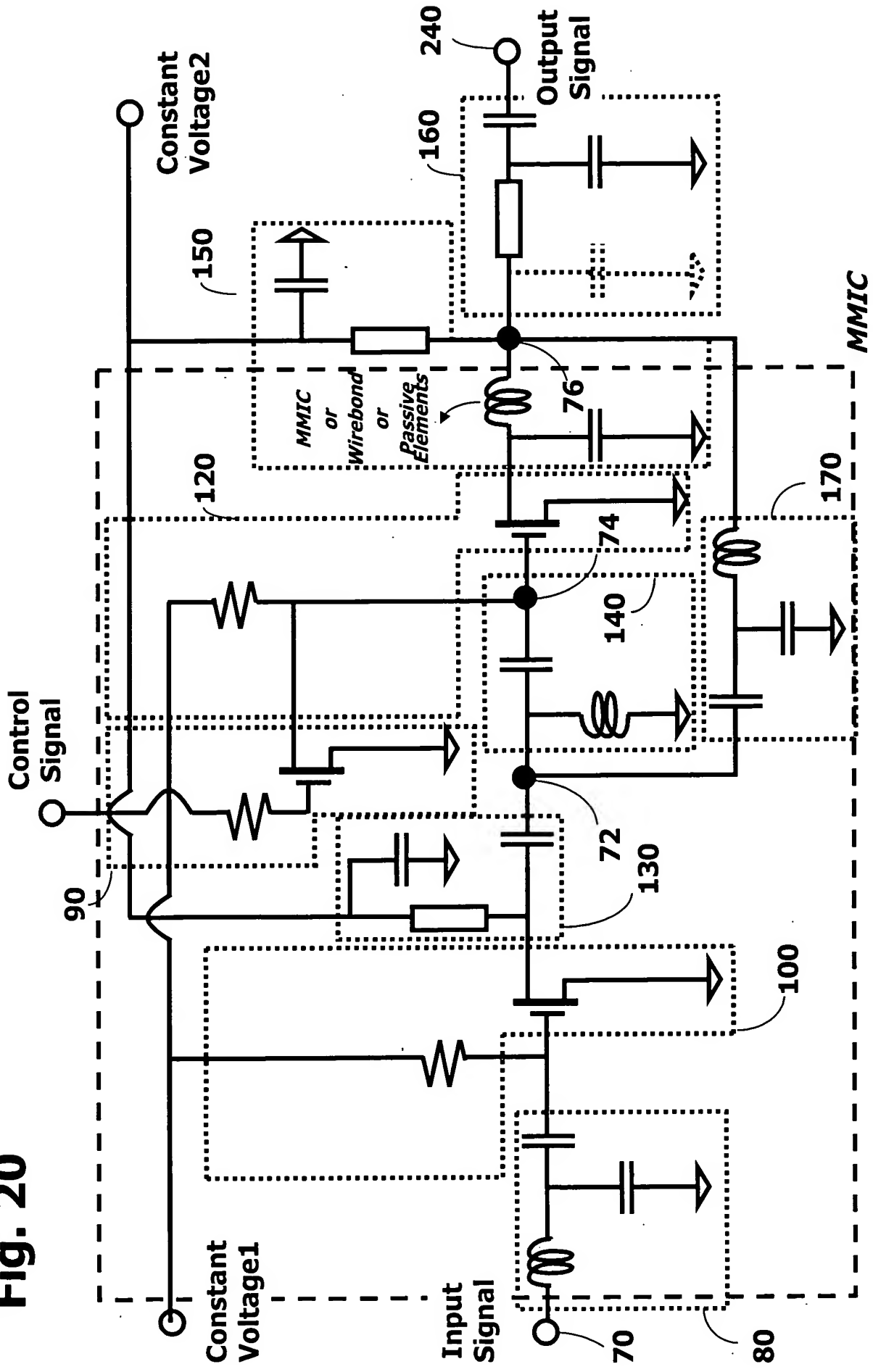

Constant Voltage2
240
Output Signal
160
150
MMIC
MMIC or Wirebond or Passive Elements
76
120
170
74
140
Control Signal
72
130
90
100
Constant Voltage1
Input Signal
70
80

Fig. 20

Fig. 21

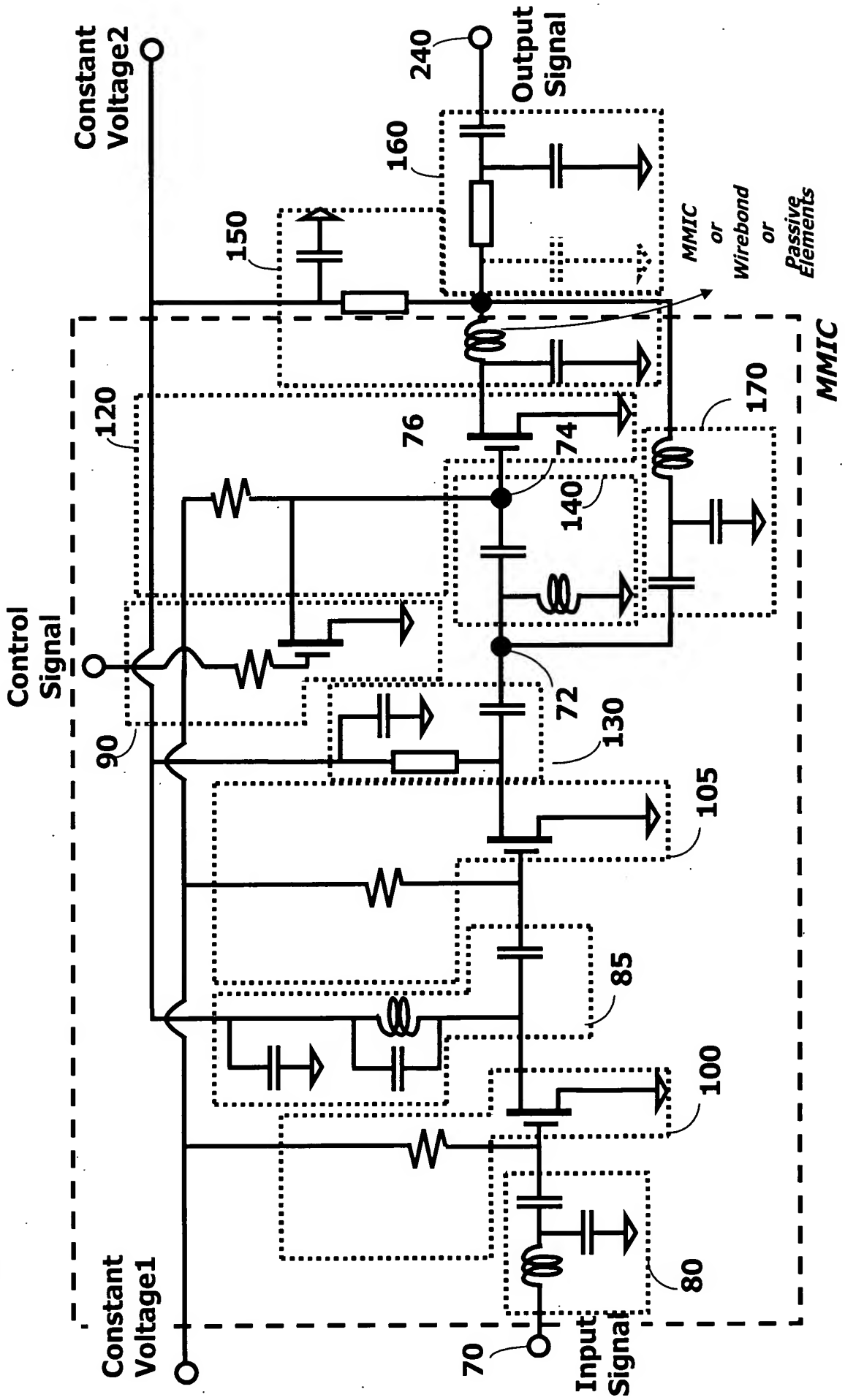

Constant Voltage2
240
Output Signal
160
150
MMIC or Wirebond or Passive Elements
MMIC
120
170
76
74
140
Control Signal
72
130
90
105
85
100
80
Constant Voltage1
70
Input Signal

Fig. 22

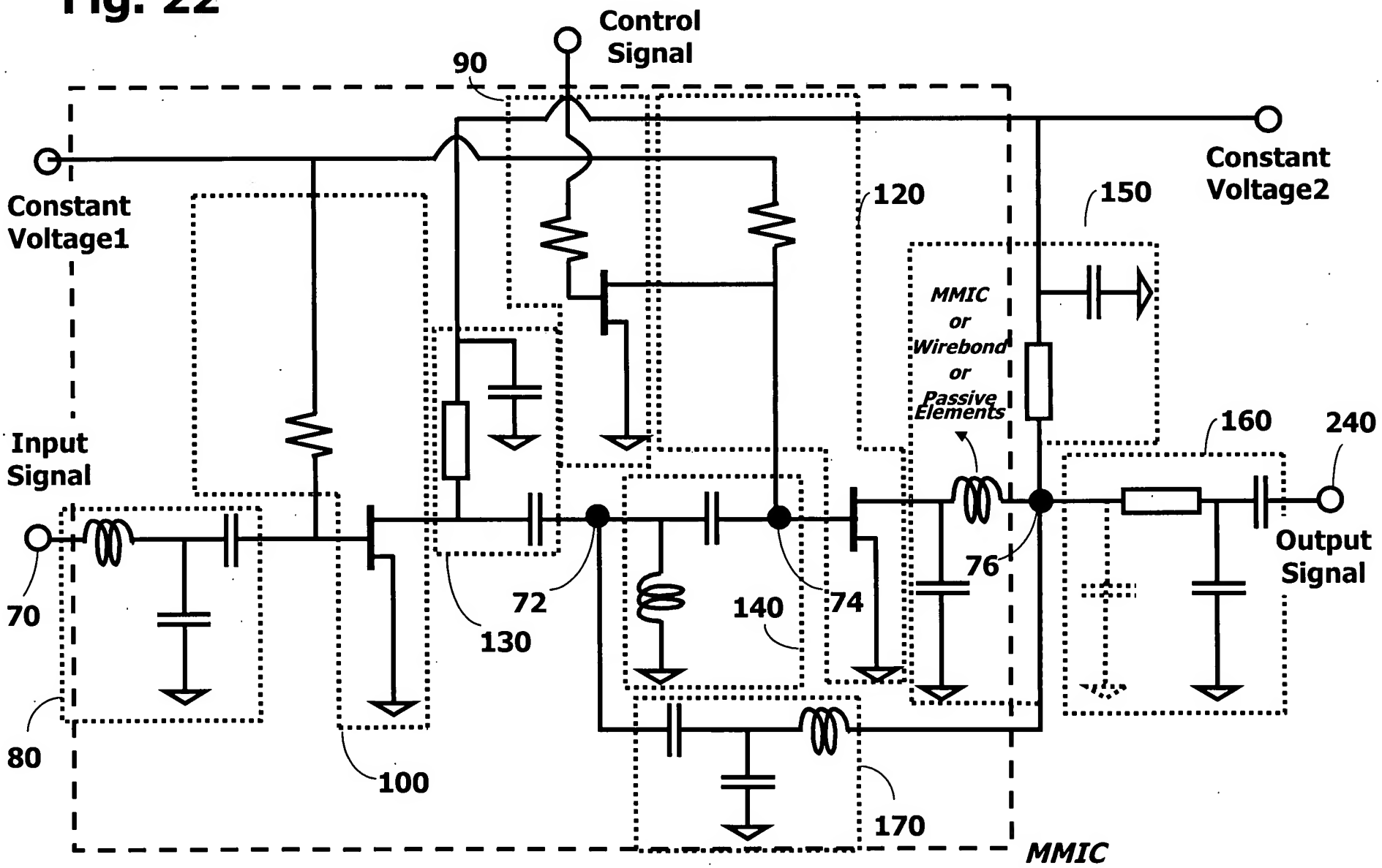

Control Signal
90
Constant Voltage1
Constant Voltage2
120
150
MMIC or Wirebond or Passive Elements
160
240
Input Signal
Output Signal
70
72
130
140
74
76
80
100
170
MMIC

Fig. 23

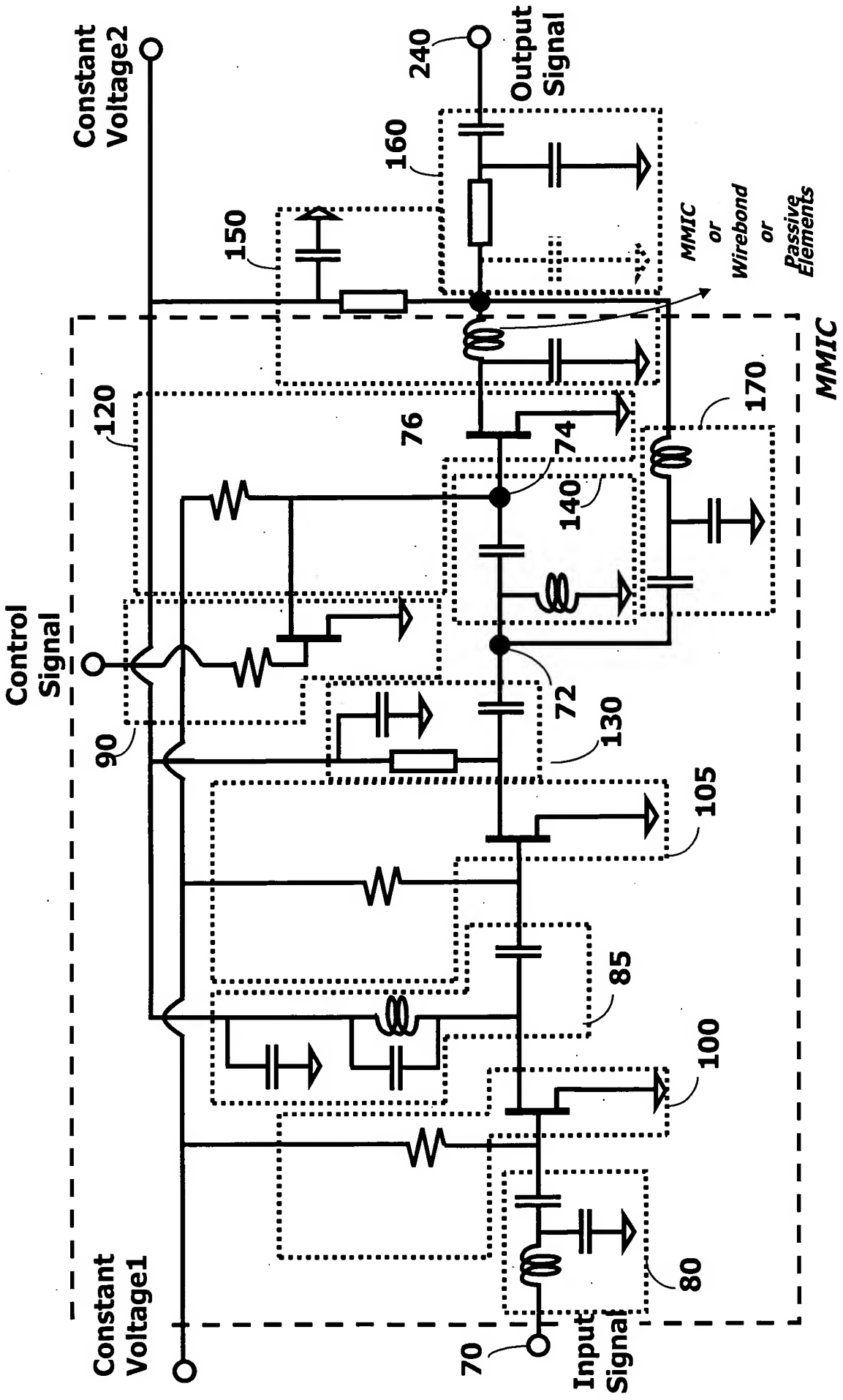

Constant Voltage2
240
Output Signal
160
150
MMIC or Wirebond or Passive Elements
MMIC
120
170
76
74
140
Control Signal
72
130
90
105
85
100
80
Constant Voltage1
70
Input Signal

Fig. 24

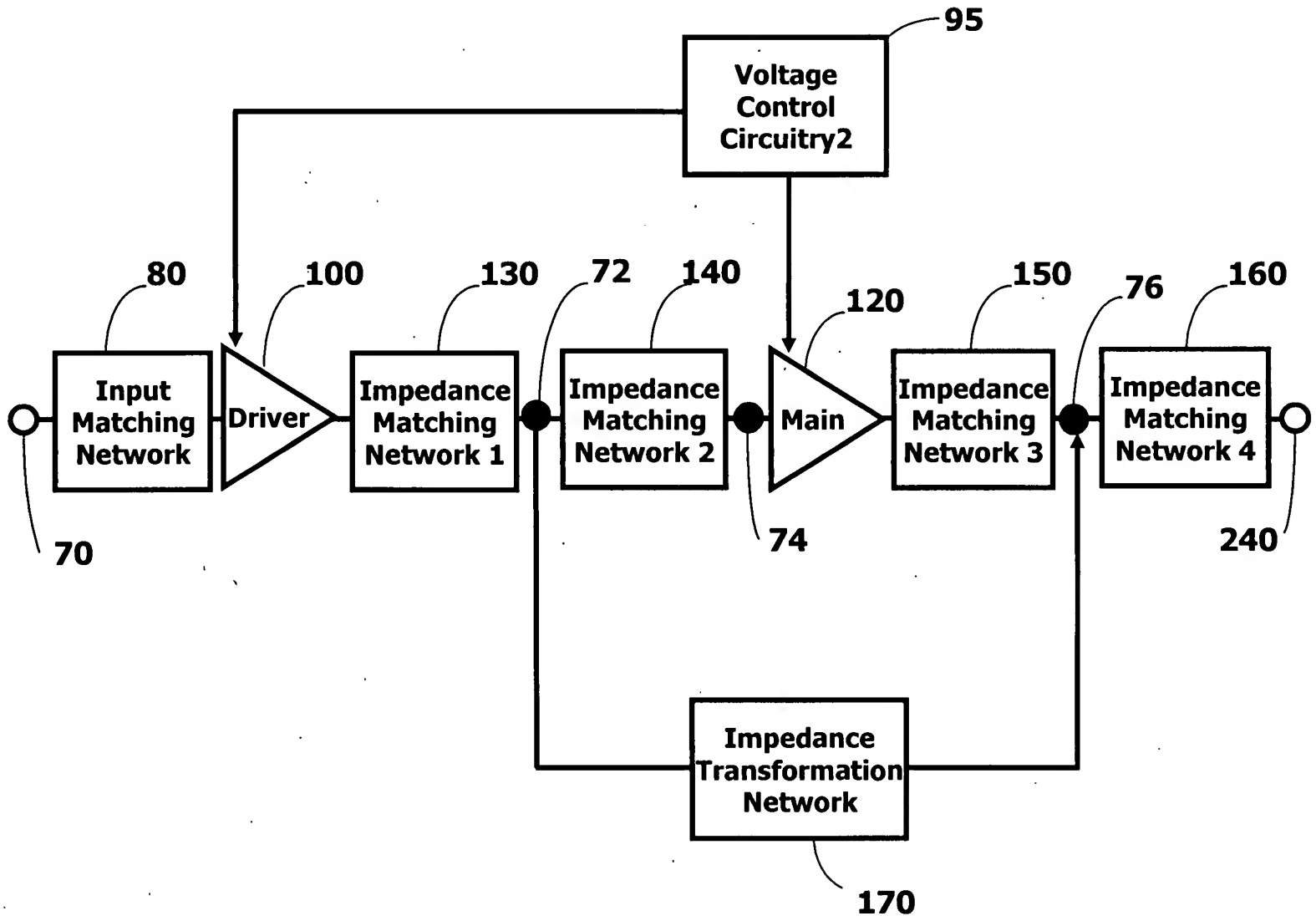
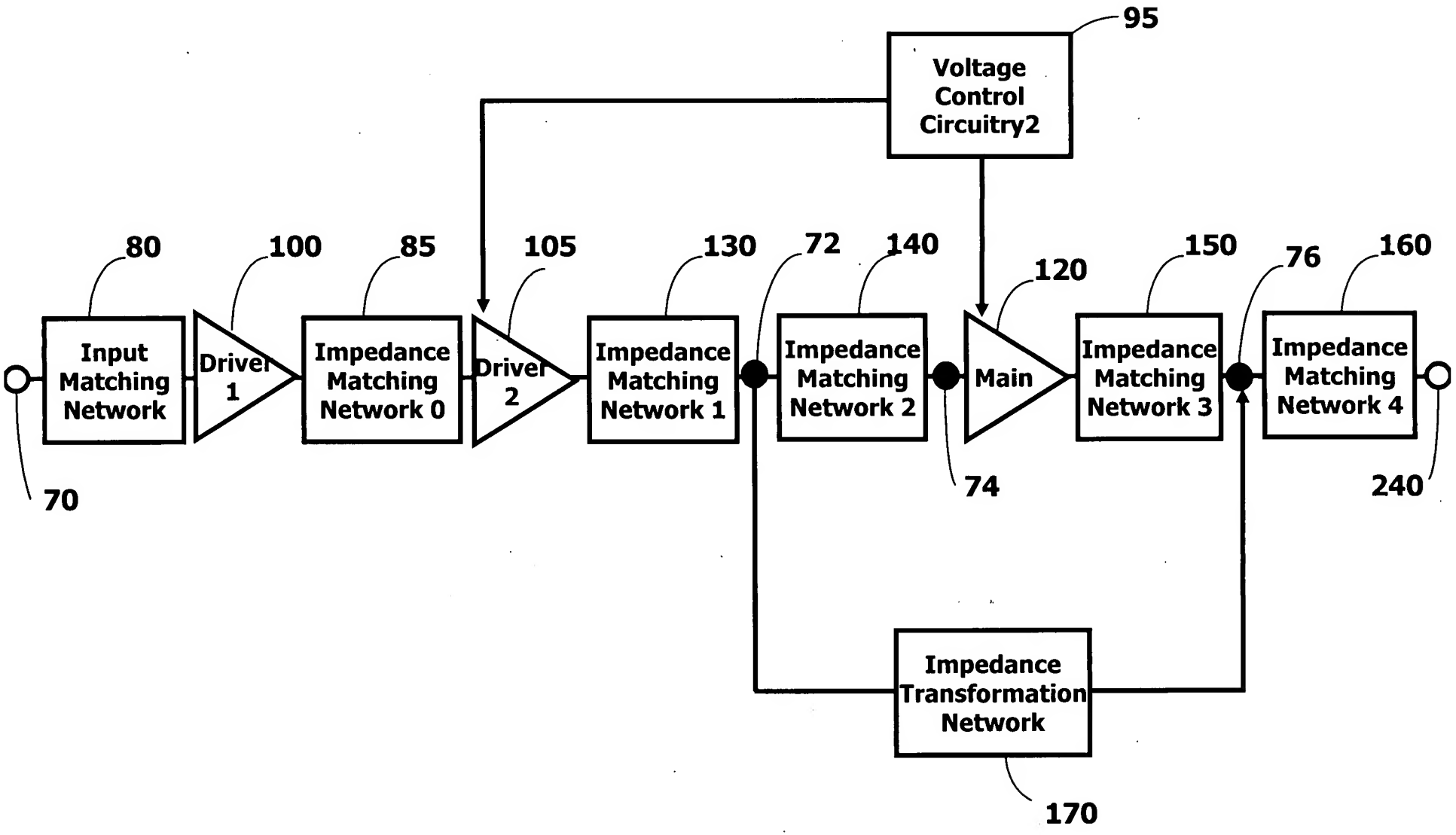

95
Voltage Control Circuitry2
80
100
130
72
140
120
150
76
160
Input Matching Network
Driver
Impedance Matching Network 1
Impedance Matching Network 2
Main
Impedance Matching Network 3
Impedance Matching Network 4
70
74
240
Impedance Transformation Network
170

Fig. 25


95
Voltage Control Circuitry2
80
100
85
105
130
72
140
120
150
76
160
Input Matching Network
Driver 1
Impedance Matching Network 0
Driver 2
Impedance Matching Network 1
Impedance Matching Network 2
Main
Impedance Matching Network 3
Impedance Matching Network 4
70
74
240
Impedance Transformation Network
170

Voltage Control Circuitry1 (90)

→ Basic Switching PAM

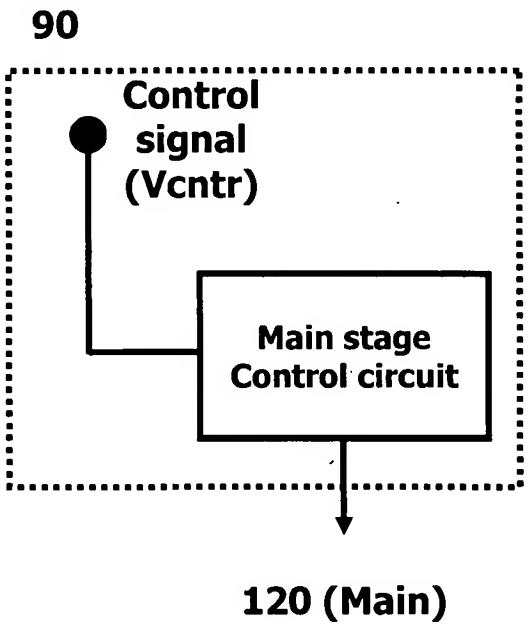


Fig. 26A

Voltage Control Circuitry2 (95)

→ Bias Modulated PAM

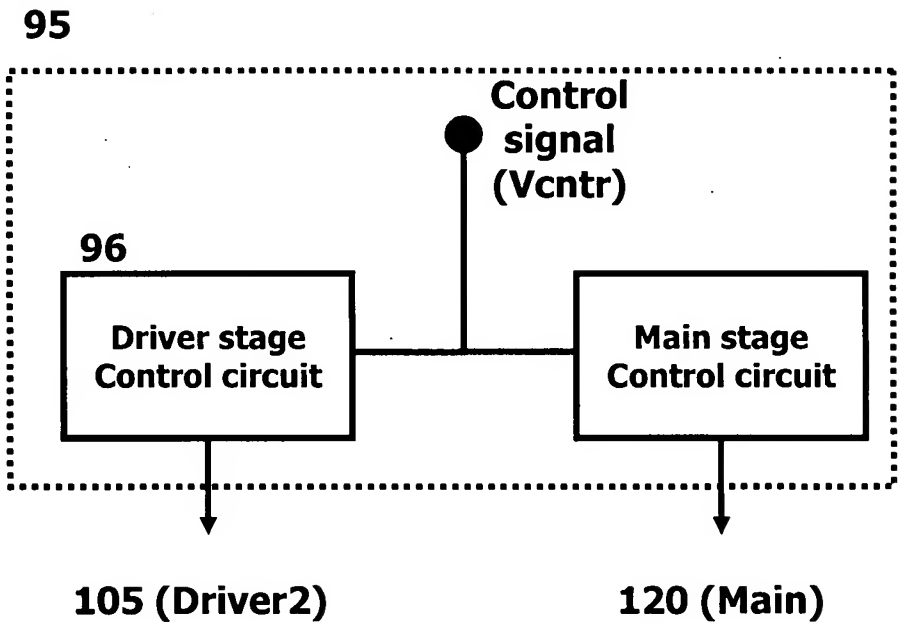


Fig. 26B

Fig. 27

Augmented voltage Control Circuitry2 (95) for Bias Modulated PAM

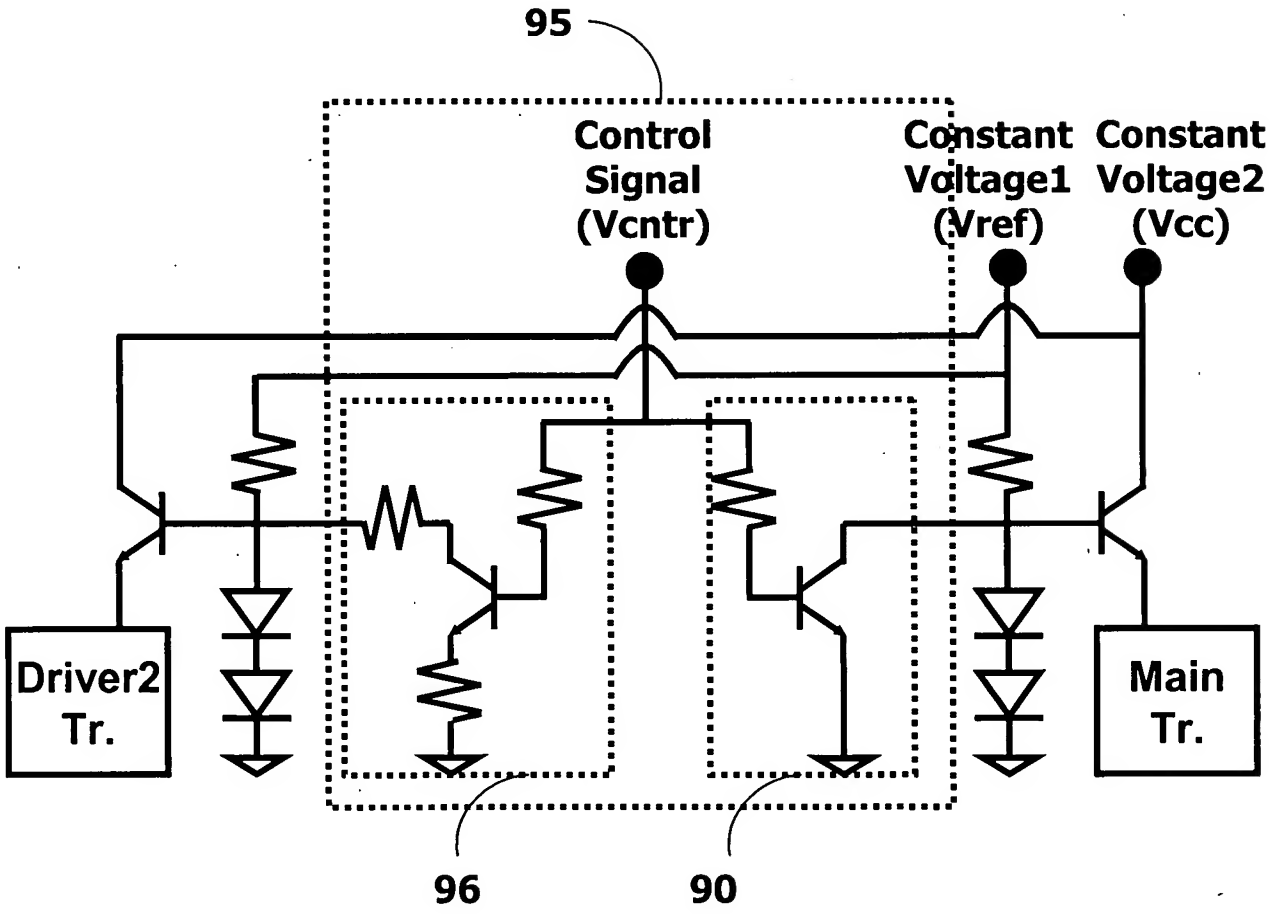
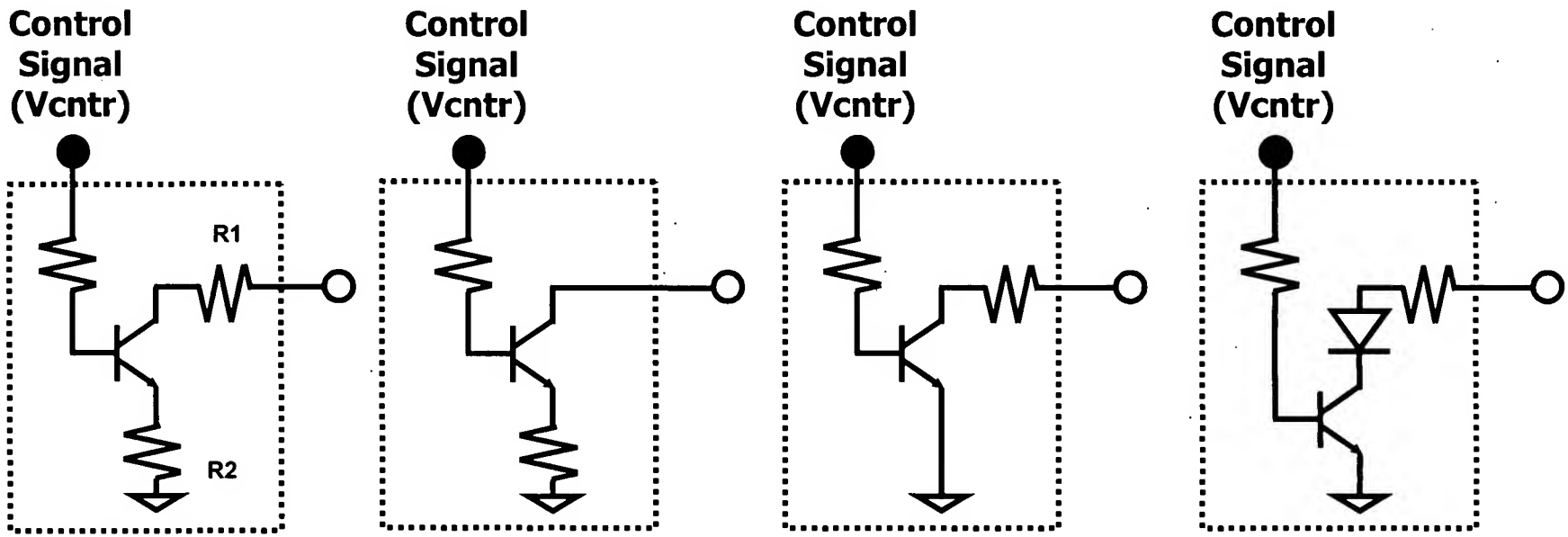


Fig. 28

Examples of Driver stage Control Circuitry (96)



28-1 28-2 28-3 28-4

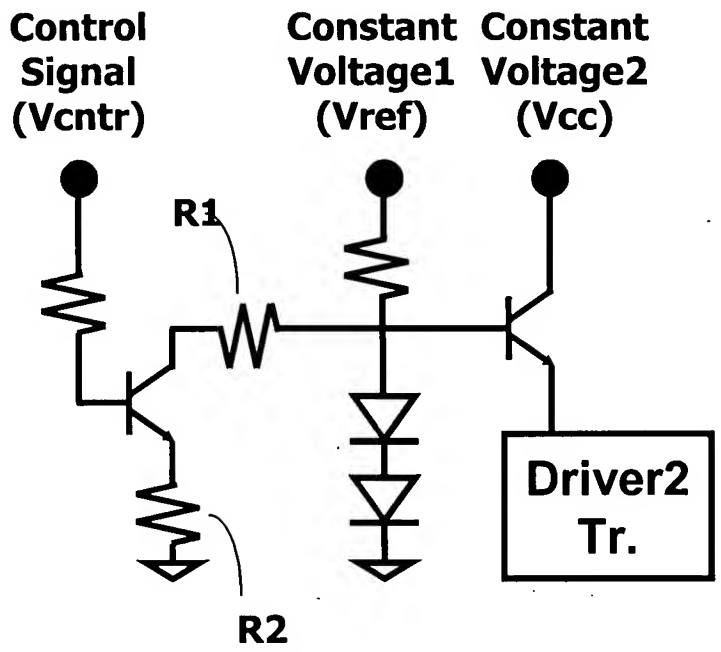


Fig. 29A

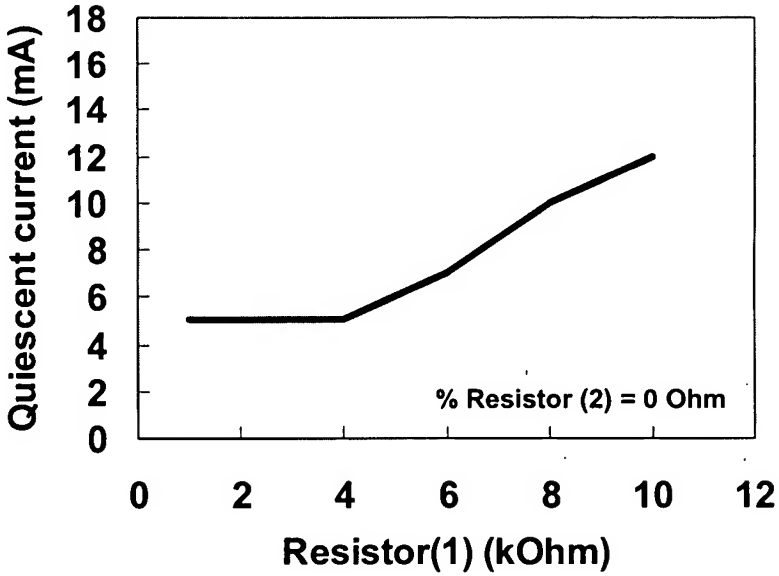


Fig. 29B

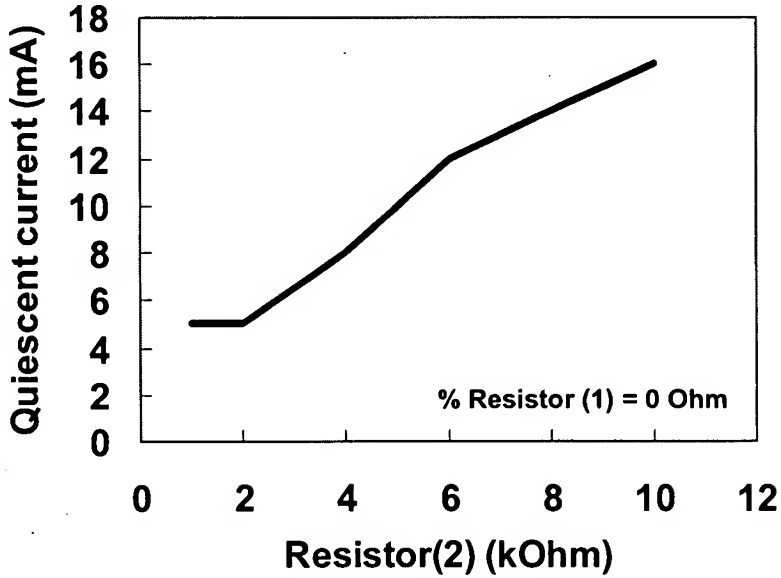


Fig. 29C

Fig. 30

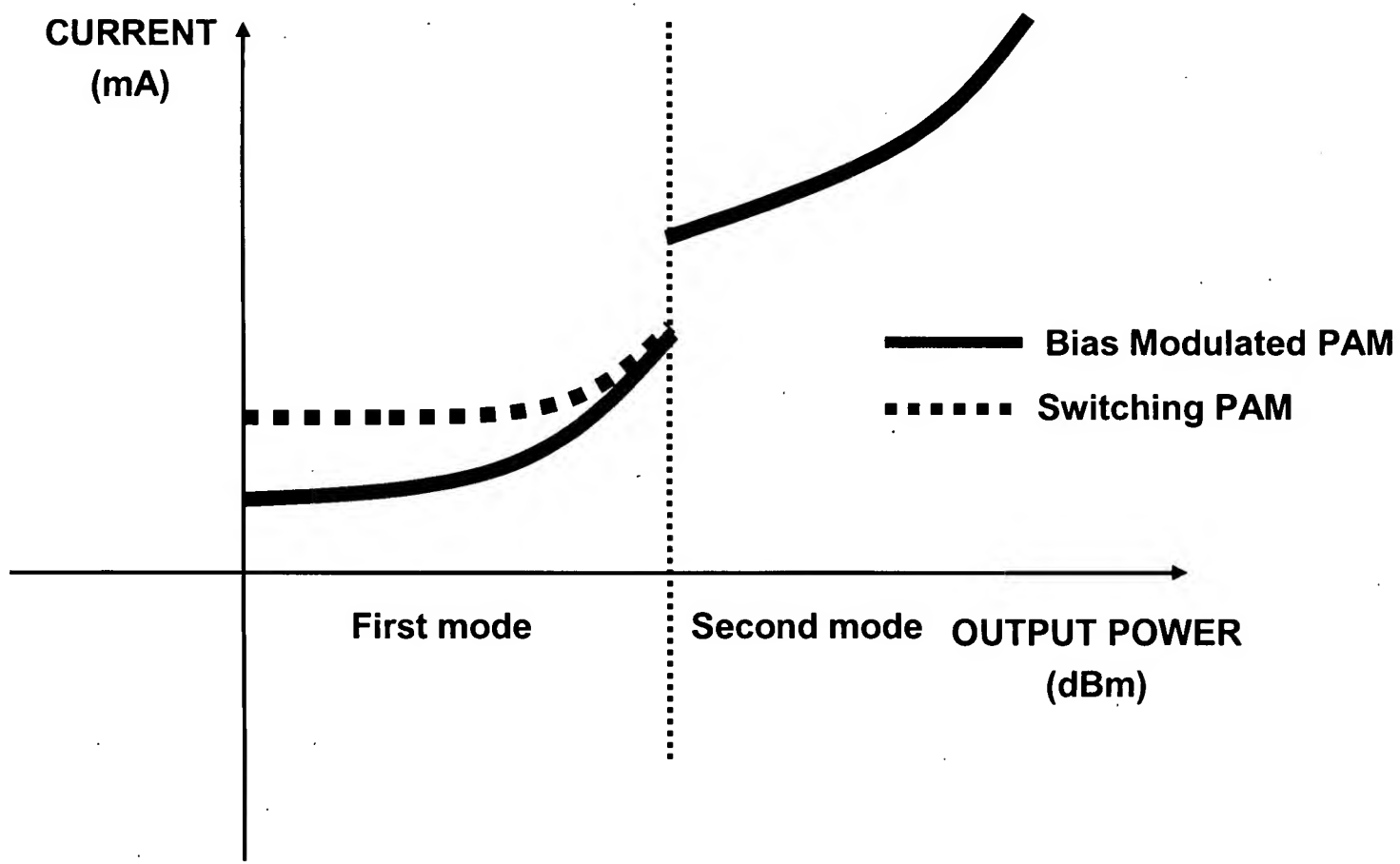

CURRENT
(mA)
Bias Modulated PAM
Switching PAM
First mode
Second mode
OUTPUT POWER
(dBm)

Fig. 31

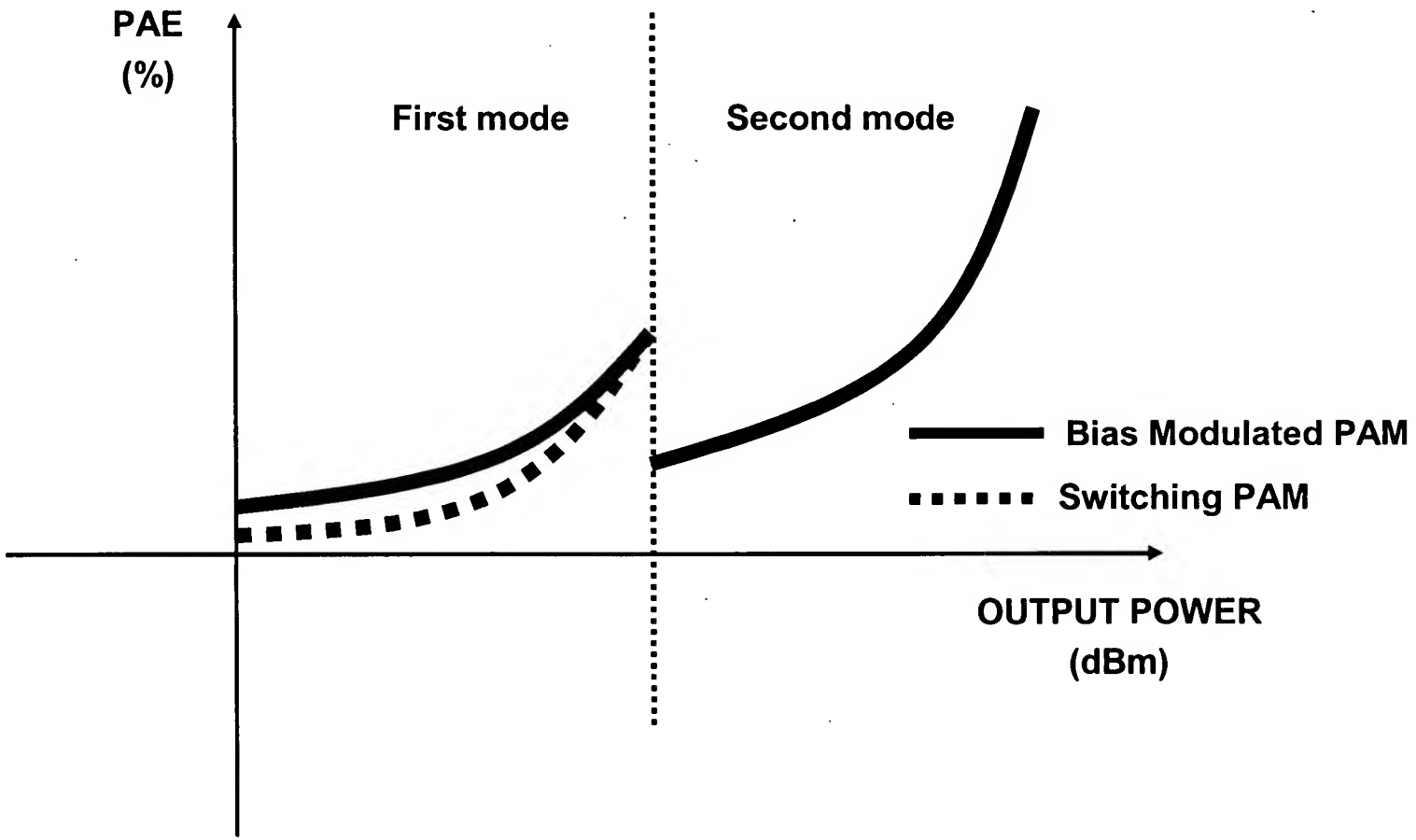

PAE
(%)
First mode
Second mode
Bias Modulated PAM
Switching PAM
OUTPUT POWER
(dBm)

Fig. 32

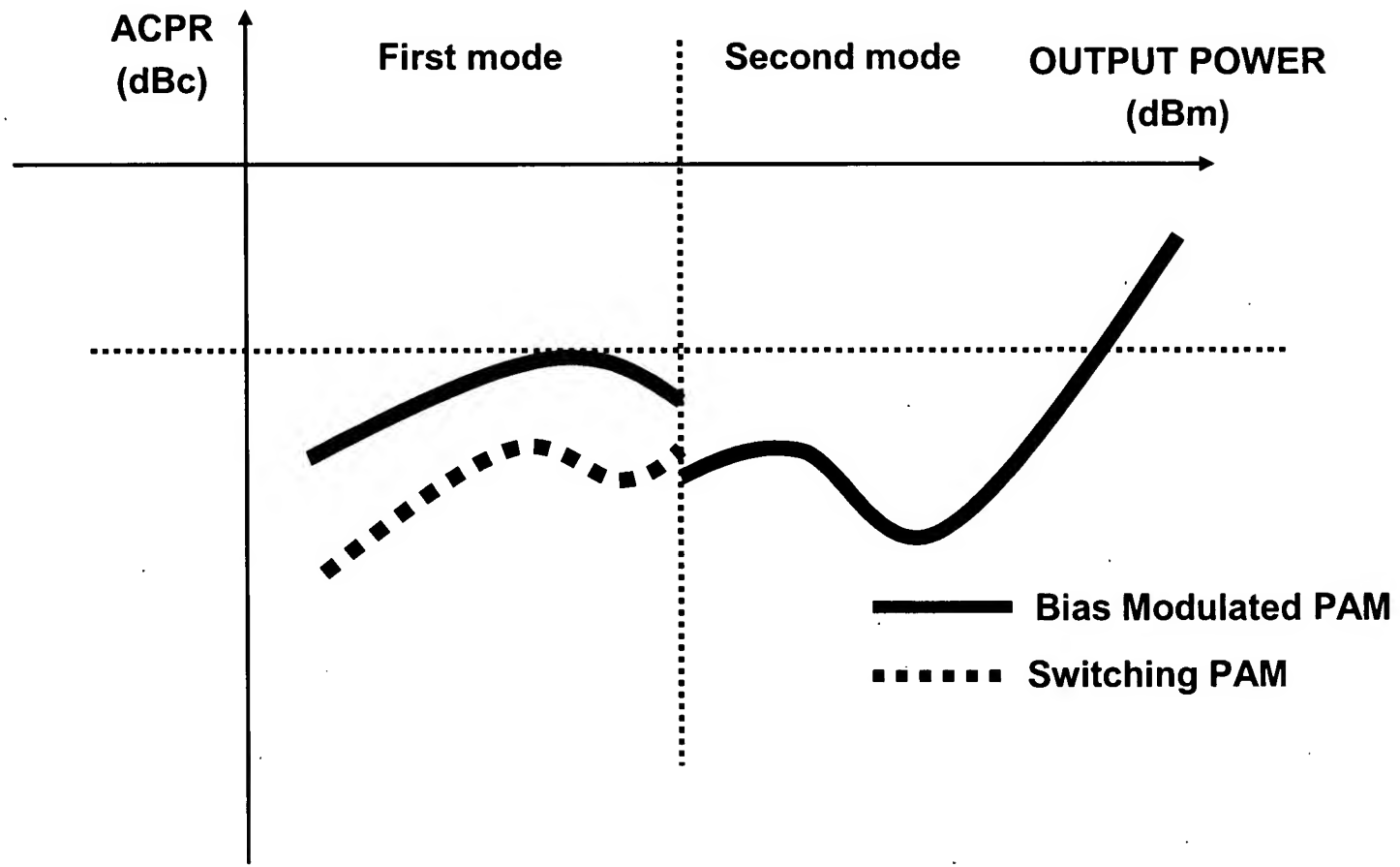
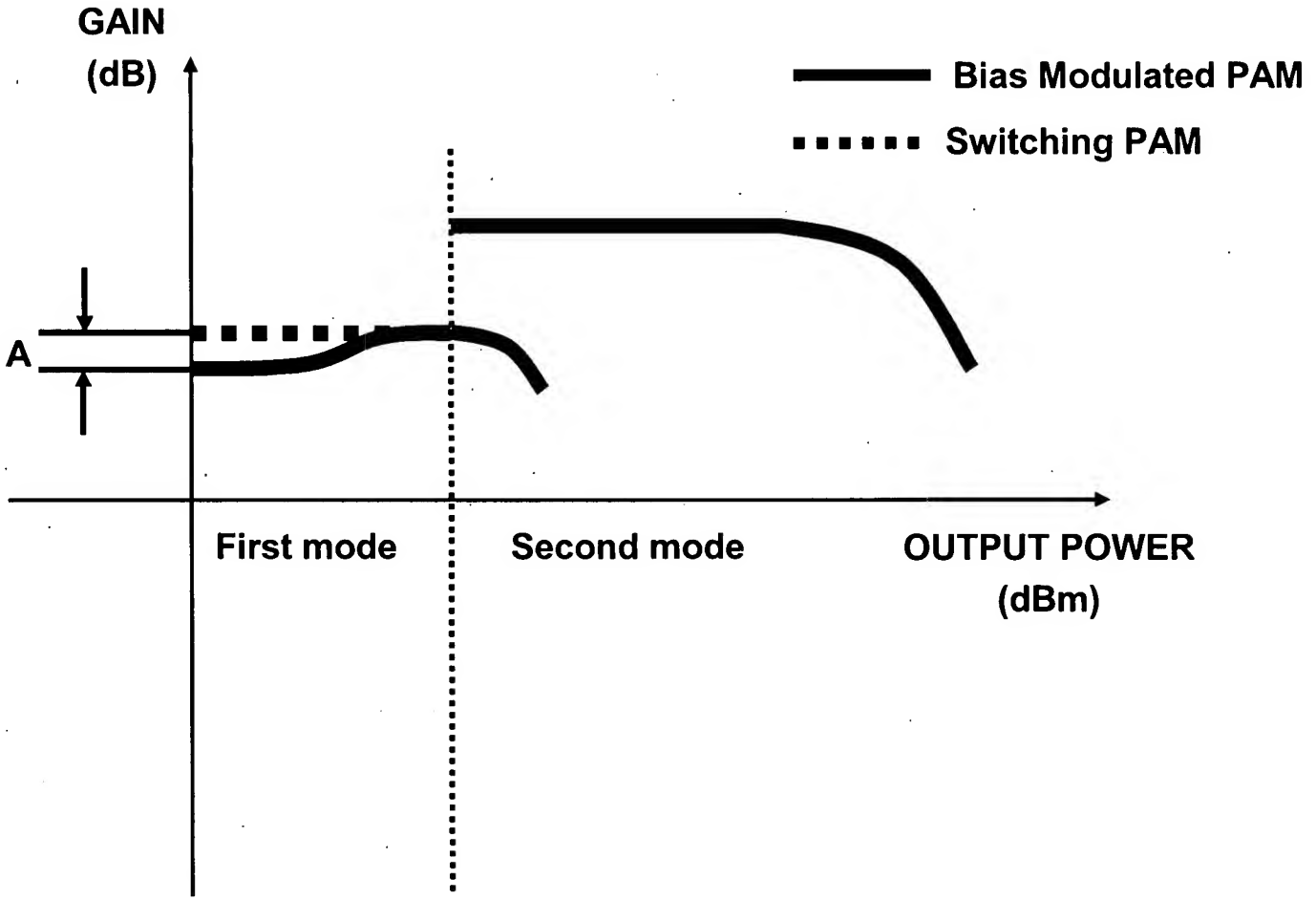

ACPR
(dBc)
First mode
Second mode
OUTPUT POWER
(dBm)
Bias Modulated PAM
Switching PAM

Fig. 33


GAIN
(dB)
Bias Modulated PAM
Switching PAM
A
First mode
Second mode
OUTPUT POWER
(dBm)